

Strike

A02 Build

MS14
2010.12.15

1. Schematic Page Description :

MS14 Schematic Ver :A01

| | | | |
|-----------------------------|----------------------------|-----------------------|----------------------------|
| 01. Title | 16. Processor_DDR3 | 31. PCH_GND | 46. N12M/DACA/DACB |
| 02. Schematic Page DESCR | 17. Processor_Power | 32. KBC_IT8518E | 47. N12M/IFPAB/IFPCD/IFPEF |
| 03. Block Diagram | 18. Processor_Power | 33. CRT | 48. N12M/I2C/THERM |
| 04. Power Block Diagram | 19. Processor_GND | 34. WEB_CAM/LVDS | 49. N12M/STARP/OSC |
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| 06. PWR_Adaptor in/Charge | 21. DDR3 SDRAM SO-DIMM 0/1 | 36. HDD/ODD | 51. GPU Power-1 |
| 07. PWR_CPU Core Power | 22. DDR3 SDRAM SO-DIMM 1/1 | 37. CARD_READER | 52. GPU Power-2 |
| 08. PWR_1.5V/1.5VS/DDR_PWR | 23. PCH_RTC,SATA,SPI,IHDA | 38. Audio_ALC269Q | 53. USB_Board |
| 09. PWR_1.05V/0.85V | 24. PCH_PCI_e,I2C,CLK | 39. AUDIO CNN | 54. LAN_RTL8111E |
| 10. PWR_5VLA/3VLA/5VA | 25. PCH_DMI,FDI,Power_CTRL | 40. Charge USB | 55. USB CNN |
| 11. PWR_1.8VS/3VS/5VS | 26. PCH_LVDS,CRT,HDMI | 41. LED | 56. PWR_SW_Board |
| 12. PWR_5VA/SCREW/IO CNN | 27. PCH_USB | 42. I/O CNN | 57. PWR_SW CNN |
| 13. POWER SEQUENCE | 28. PCH_GPIO,MISC | 43. WLAN,BT | 58. GP_Board |
| 14. Processor_DMI,FDI,PCI_e | 29. PCH_POWER | 44. N12M/PCI-EXPRESS | 59. GP CNN |
| 15. Processor_THRM,MISC | 30. PCH_POWER | 45. N12M/FRAME_BUFFER | |

2. PCI & IRQ & DMA Description :

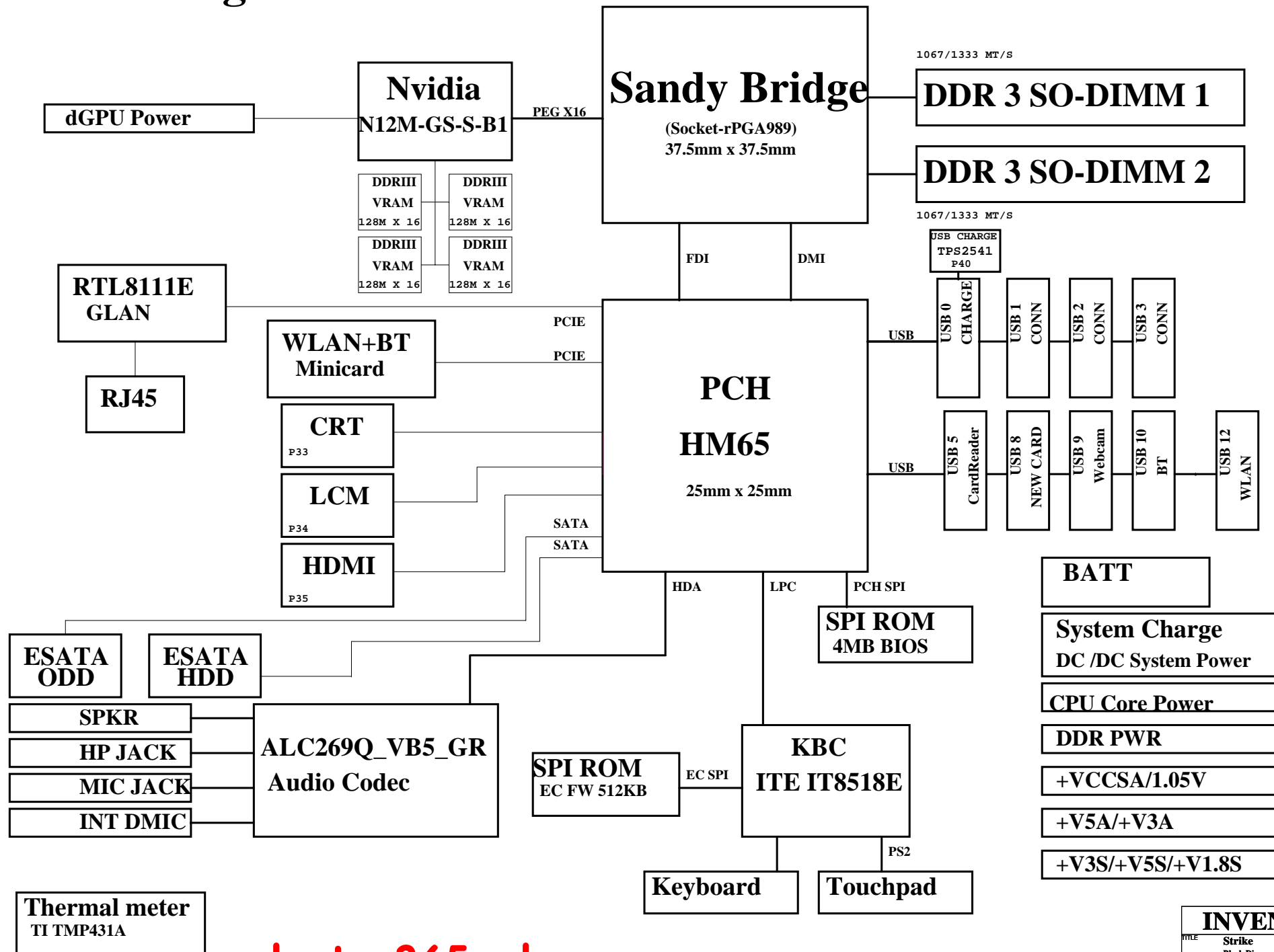
| | | | | | | |
|-------|------|--------|------|-----------|------|------|
| IDSEL | CHIP | PCIINT | CHIP | Interface | REQ | CHIP |
| None | | None | | | None | |

3. USB & PCI-Express & SATA Description :

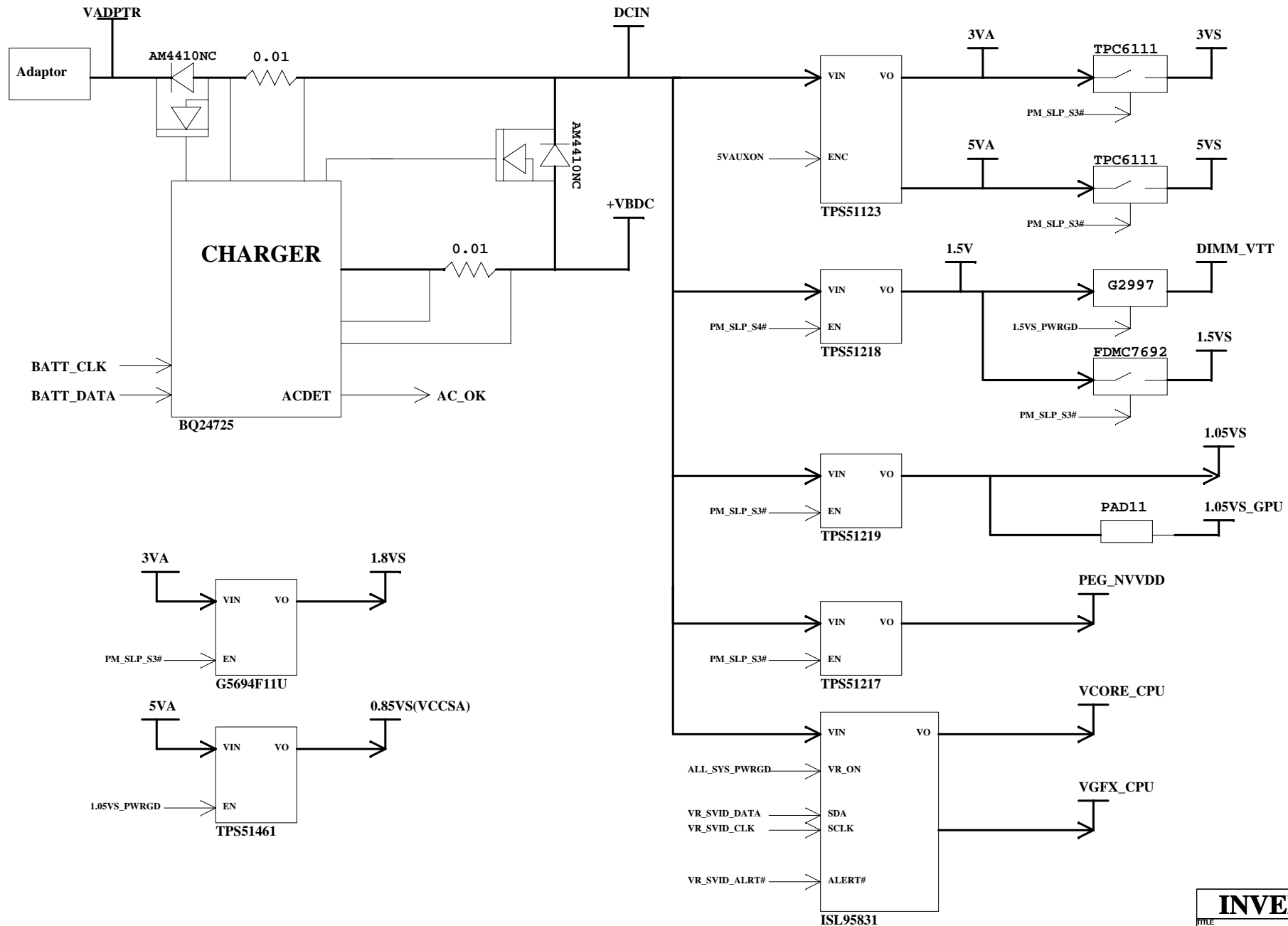
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|----------|-------------|----------|-----------|--------|--------|--------|--------|
| USB Port | DEVICE | USB Port | DEVICE | PCI-E | DEVICE | SATA | DEVICE |
| Port 0 | Charge Port | Port 7 | | Port 1 | WLAN | Port 1 | HDD |
| Port 1 | System | Port 8 | | Port 2 | | Port 2 | |
| Port 2 | System | Port 9 | Web Cam | Port 3 | LAN | Port 4 | ODD |
| Port 3 | System | Port 10 | Bluetooth | Port 4 | | Port 5 | |
| Port 4 | | Port 11 | | Port 5 | | | |
| Port 5 | CardReader | Port 12 | WLAN | Port 6 | | | |
| Port 6 | | Port 13 | | | | | |

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3. Block Diagram :



Power Block Diagram :



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| INVENTEC | | | |
|---------------------|------|------------|-------|
| Strike | | | |
| Power Block Diagram | | | |
| SIZE | CODE | DOC NUMBER | REV |
| C | CS | CS-131 | A02 |
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4. Net name Description :

Voltage Rails

| | |
|---------------|--|
| DCIN | Primary DC system power supply |
| 3VLA | 3.3V always on power rail by DCIN |
| 5VLA | 5.0V always on power rail by DCIN |
| EC_3VLA | 3.3V always on power rail by 5VAUXON |
| 3VA | 3.3V always on power rail by LATCH_ON |
| 5VA | 5.0V always on power rail by LATCH_ON |
| 3VM | 3.3V power rail by SUSM# |
| 1.05VM | 1.05V switched power rail by SUSM# |
| 1.5V | 1.5V switched power rail by SUSC# |
| 1.8V | 1.8V power rail by SUSC# |
| 3VS | 3.3V power rail by SUSB# |
| 5VS | 5.0V power rail by SUSB# |
| 1.5VS | 1.5V power rail by SUSB# |
| 1.05VS | 1.05V power rail by SUSB# |
| PWR_DIMM_VTT | 0.75V DDR Termination Voltage by SUSB# |
| VGFX_CORE | 1.05V power rail for UMA by SUSB# |
| PEG_1.8VS | 1.8V switched power rail for NB9x by SUSB# |
| PEG_PEX_1.1VS | 1.1V switched power rail for NB9x by SUSB# |
| PEG_NVDD | Variable switched power rail for NB9x by SUSB# |
| Vcore_CPU | Core switched power rail for CPU |

Part Naming Conventions




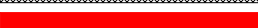




| | | | |
|----|-------------|----|--------------------------|
| C | = Capacitor | Q | = Transistor |
| CN | = Connector | R | = Resistor |
| D | = Diode | RP | = Resistor Pack |
| F | = Fuse | U | = Arbitrary Logic Device |
| L | = Inductor | Y | = Crystal and Osc |

Name Suffix

| | |
|----|---------------------|
| # | = Active Low signal |
| NU | = No Stuff |

5. Board Stack up Description

PCB Layers

| | | |
|---------|---|---|
| Layer 1 |  | Component Side, Microstrip signal Layer |
| Layer 2 |  | Ground Plane |
| Layer 3 |  | Stripline Layer |
| Layer 4 |  | Power Plane |
| Layer 5 |  | Stripline Layer |
| Layer 6 |  | Stripline Layer |
| Layer 7 |  | Ground Plane |
| Layer 8 |  | Solder Side, Microstrip signal Layer |

| | Differential Impedance for Microstrip(5-mils) | Differential Impedance for Stripline(4-mils) |
|-------------|---|--|
| Host Clock | 95 ohm +/- 20% | 100 ohm +/- 20% |
| PCI-E Clock | 95 ohm +/- 20% | 100 ohm +/- 20% |
| DDR2 CLK | 70 ohm +/- 20% | 70 ohm +/- 20% |
| DDR2 Strobe | 85 ohm +/- 20% | 90 ohm +/- 20% |
| DMI Bus | 95 ohm +/- 20% | 100 ohm +/- 20% |
| PCI-E Bus | 95 ohm +/- 20% | 100 ohm +/- 20% |
| SDVO | 95 ohm +/- 20% | 100 ohm +/- 20% |
| SATA | 95 ohm +/- 20% | 100 ohm +/- 20% |
| USB | 90 ohm +/- 20% | 95 ohm +/- 20% |
| LVDS | 100 ohm +/- 20% | 100 ohm +/- 20% |
| Lan | 95 ohm +/- 20% | 100 ohm +/- 20% |

| Power Rail | Destination | Voltage | S0 Current |
|-----------------------------------|---|--|---|
| VCC_CORE | Penryn HFM: LFM: | 1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V | 36A |
| 1.05VS | Penryn: AGTL+ termination Cantiga GM: Core Cantiga GM: PCIE Cantiga GM:Core+IMEL+HSIO Cantiga GM:VCC_GMCH Cantiga GM:VCCA_SM_CK and NCTF Cantiga GM:VCC_DMI Cantiga GM:VCCA_SM Cantiga GM:VTT ICH9M:VCC1_O5 ICH9M:DMI ICH9M:CPU_IO | 1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V | 4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA |
| 1.5VS | Penryn PLL Cantiga GM: QDAC Cantiga GM: LVDS Cantiga GM: TVDAC Cantiga GM: Various PLLS analog supply Cantiga GM: VCC_SM_CK Cantiga GM: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card: | 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V | 130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA |
| 1.5V | Cantiga GM: DDRIII System Memory | 1.425V-1.5V-1.575V | 3.1A(800M) 4.1A(1067M) |
| 0.75VDDT_DDRIIIDDRIII Terminator: | | 0.7125V-0.75V-0.7875V | 1.0A |
| 3VS | Cantiga GM: HV CMOS Cantiga GM: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS397BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC: | 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V | 105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA |
| 1.8VS | DVI | 3.0V-3.3V-3.6V | 120mA |
| 3VA | ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:82567LM Azalia MDC: Flash ROM: BIOS | 2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 1.0V and 1.8V 3.0V-3.3V-3.6V | 6uA 212mA 73mA 78mA 2A Each 1A |
| 5VS | Cardreader: GL827 Azalia Codec: ALC262 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam | 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V | Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA |
| 5VA | USB: x 2 ports USB and ESATA | 5VA 5VA | 1.5A 2A |
| 5VLA | Control Power | | |
| 3VLA | EC: ITE8512E | 3.0V-3.3V-3.6V | 300mA |

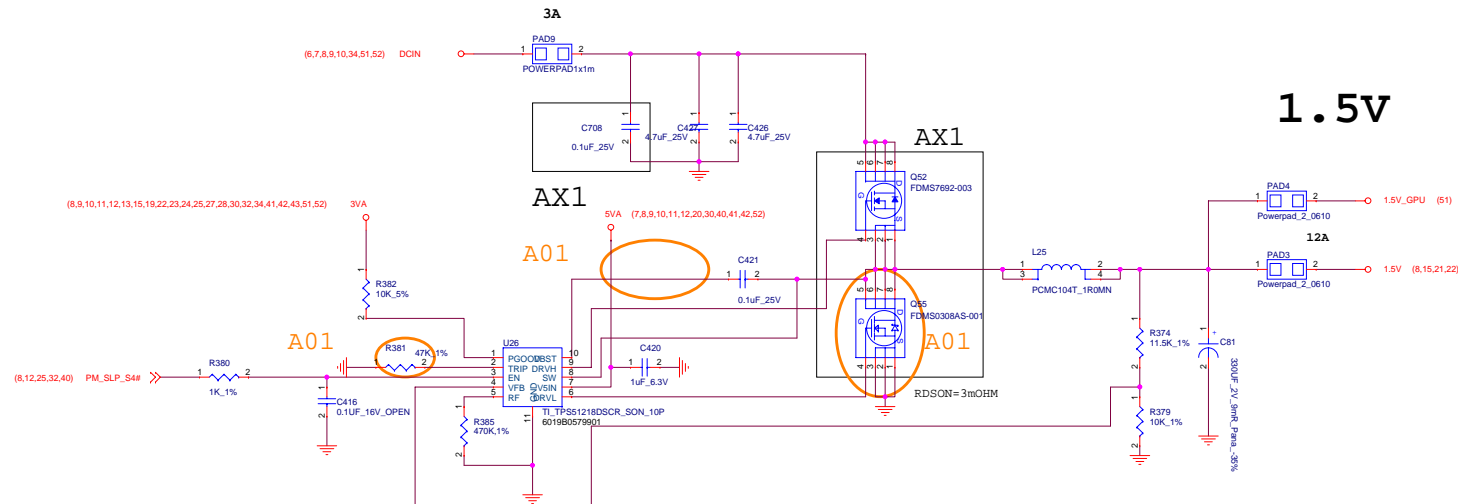
INVENTEC

Annotations

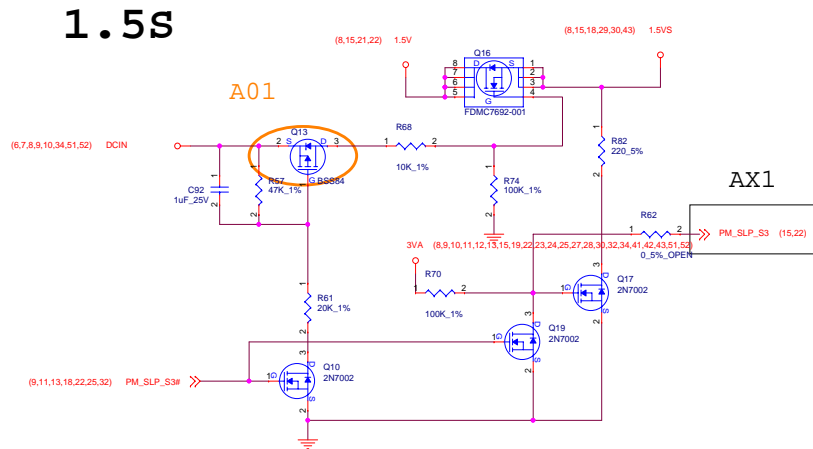
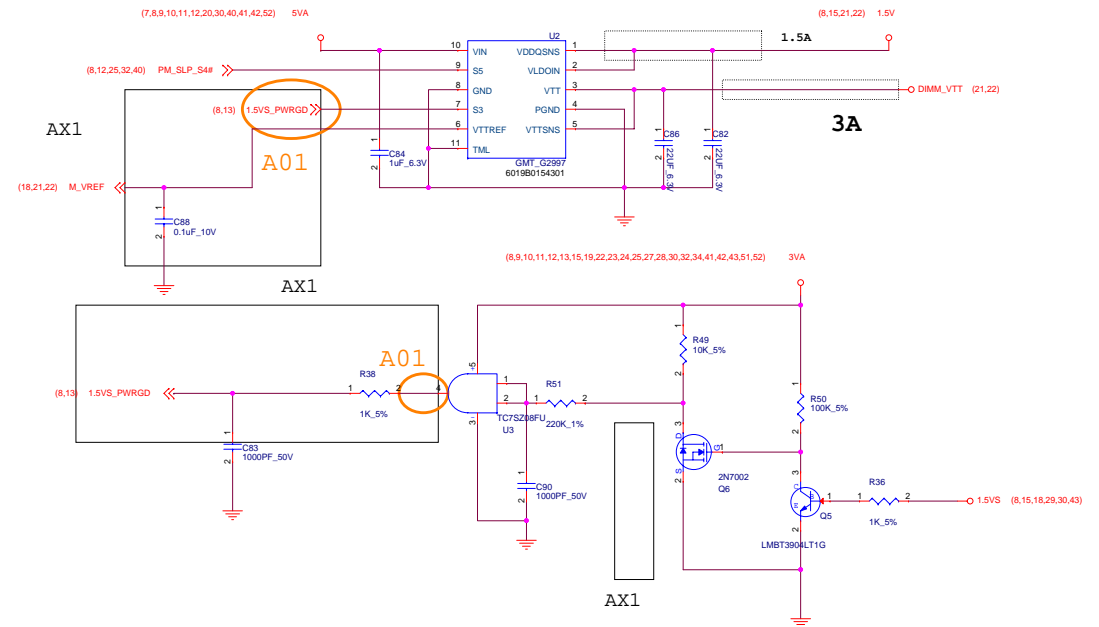
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Custom CS CS-131 5 of 39

CHANGE by IEC DATE Friday, December 17, 2010

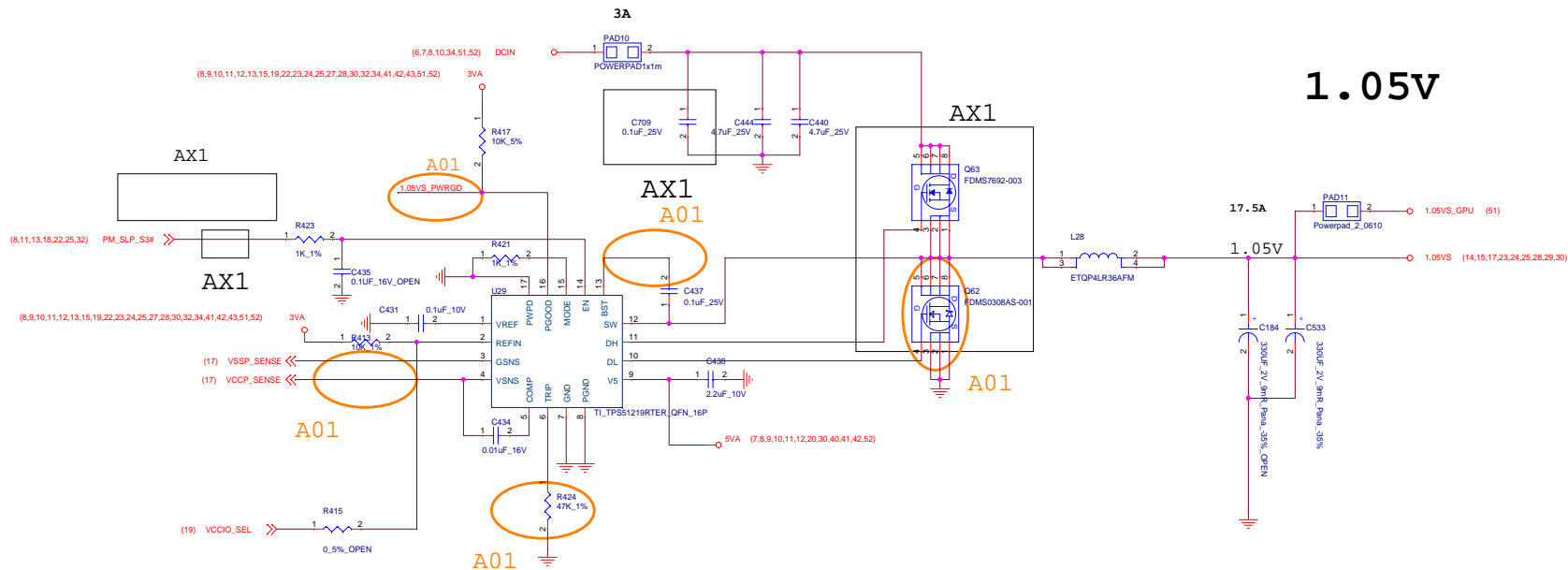
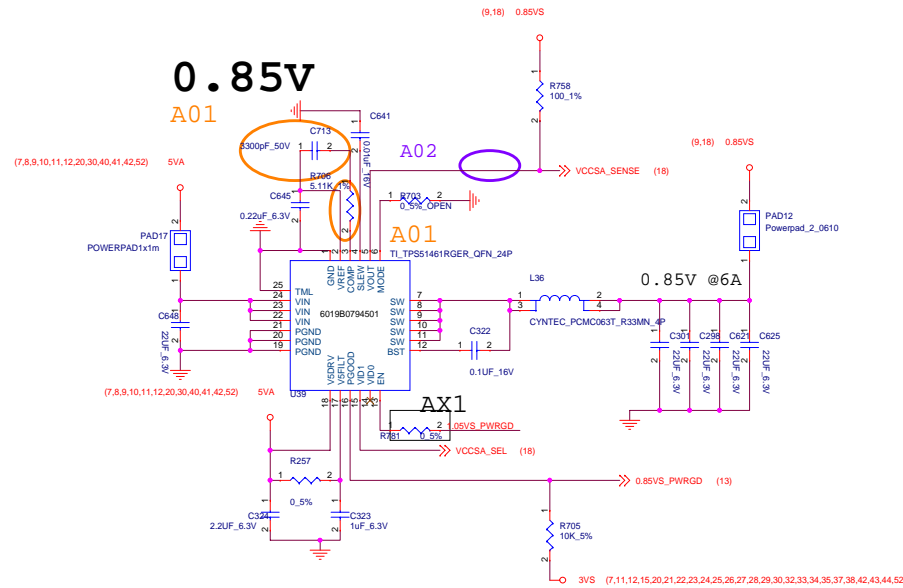
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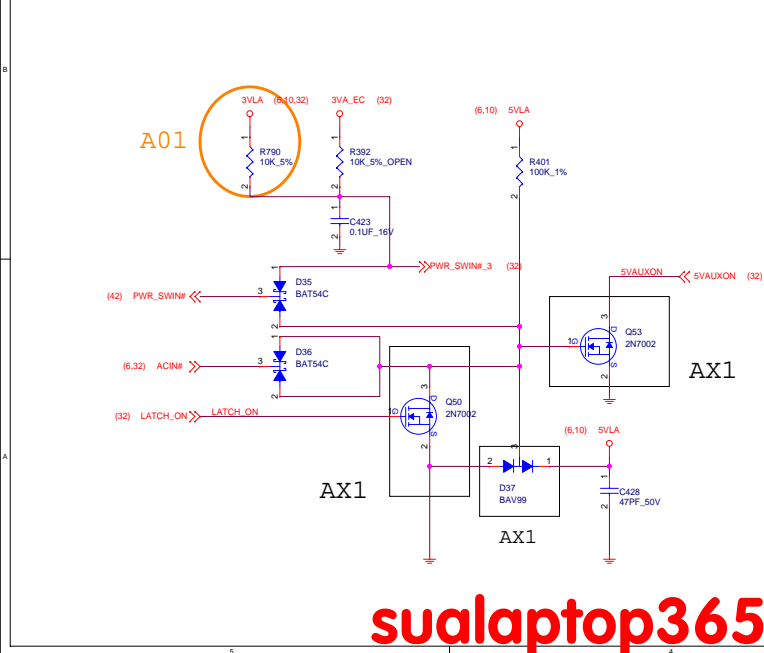
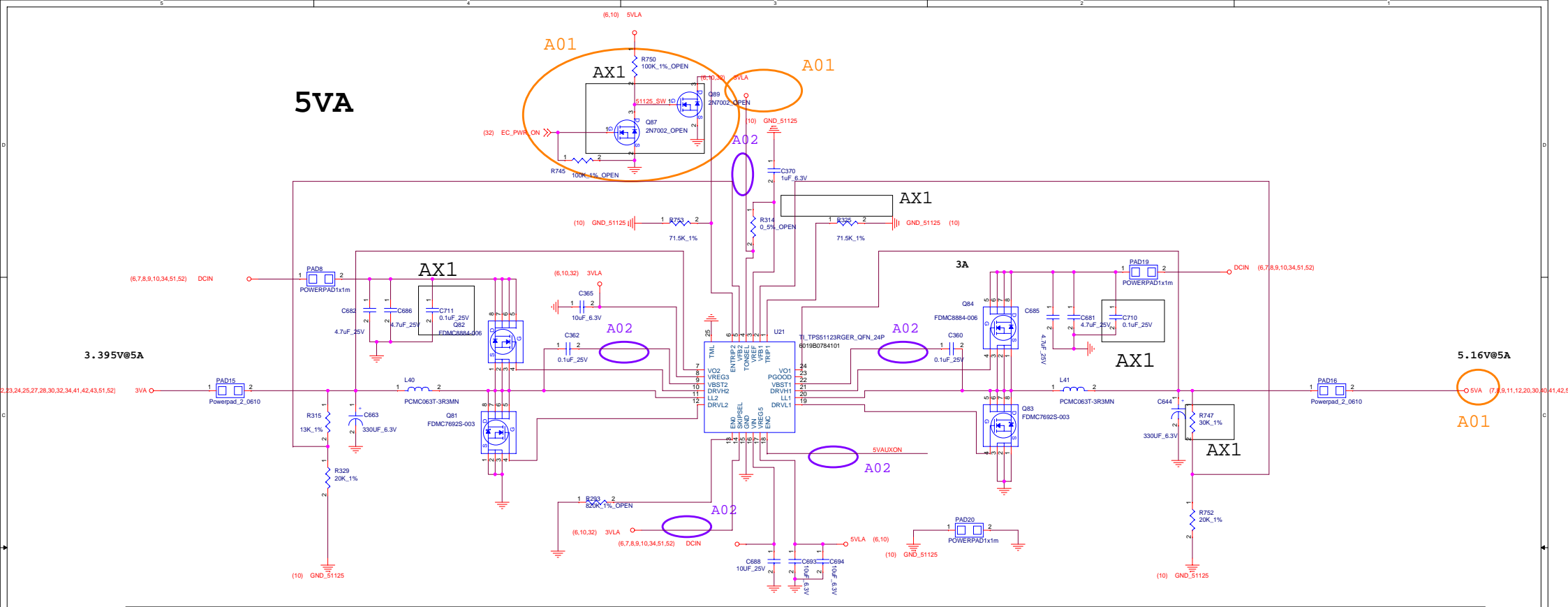


DIMM_VTT



| INVENTEC | | | | |
|--------------|------|------------|-------|--|
| TITLE Strike | | | | |
| DDR PWR | | | | |
| SIZE | CODE | DOC NUMBER | REV | |
| Custom | CS | CS-131 | A02 | |
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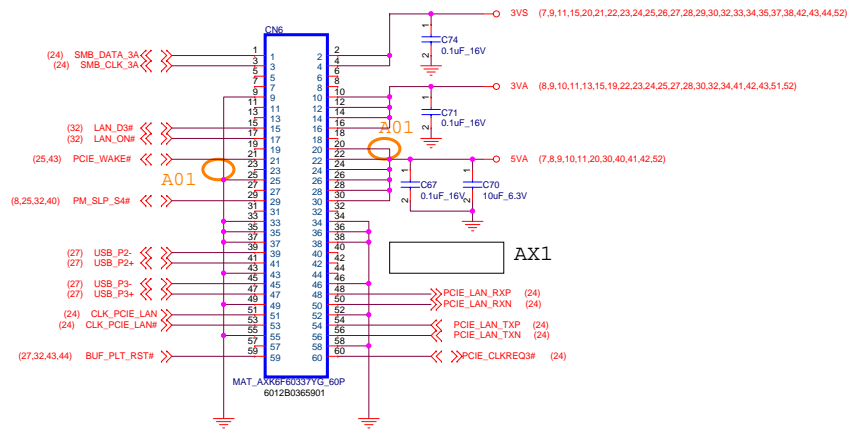




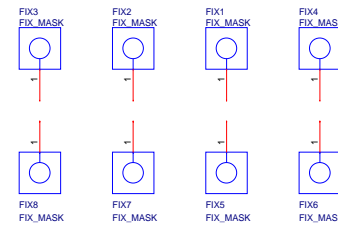
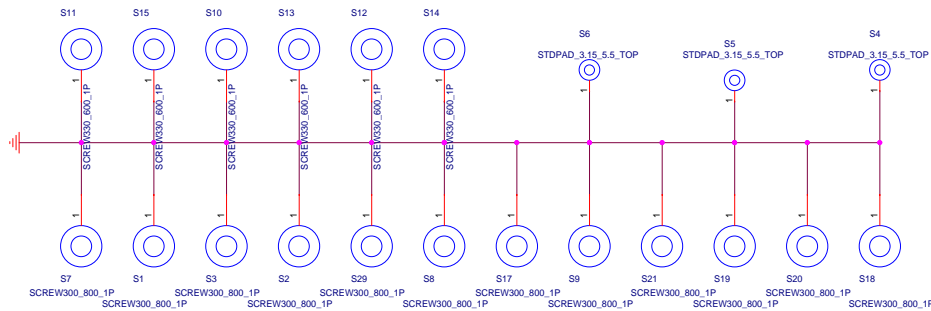
[illegible][illegible]

The schematic diagram shows a power supply circuit. The input is 5V 5A. The circuit includes a 47K 1% resistor (R285), a 220uF 10V capacitor (C352), two TPC6111 MOSFETs (Q37, Q36), a 1K 1% resistor (R305), a 2N7002 MOSFET (Q38), and a PM_SLP_S3# signal source. The output is 5V 8A. A yellow oval highlights the MOSFETs and the 2N7002 MOSFET, labeled A01.

IO CNN



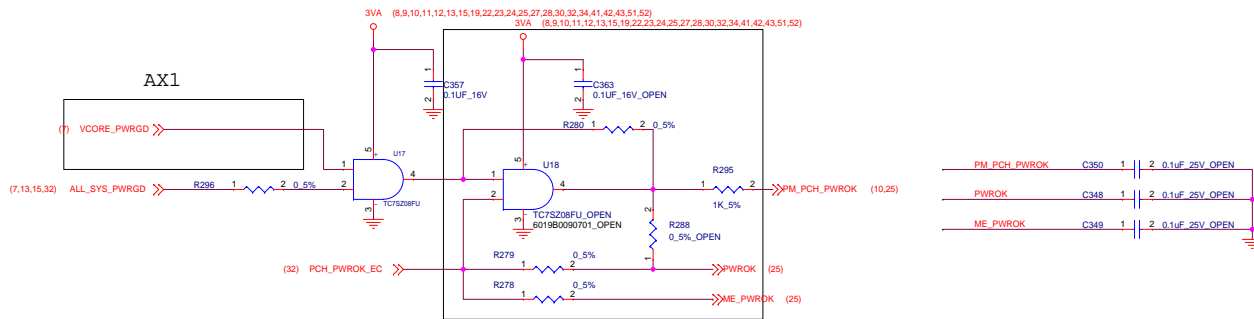
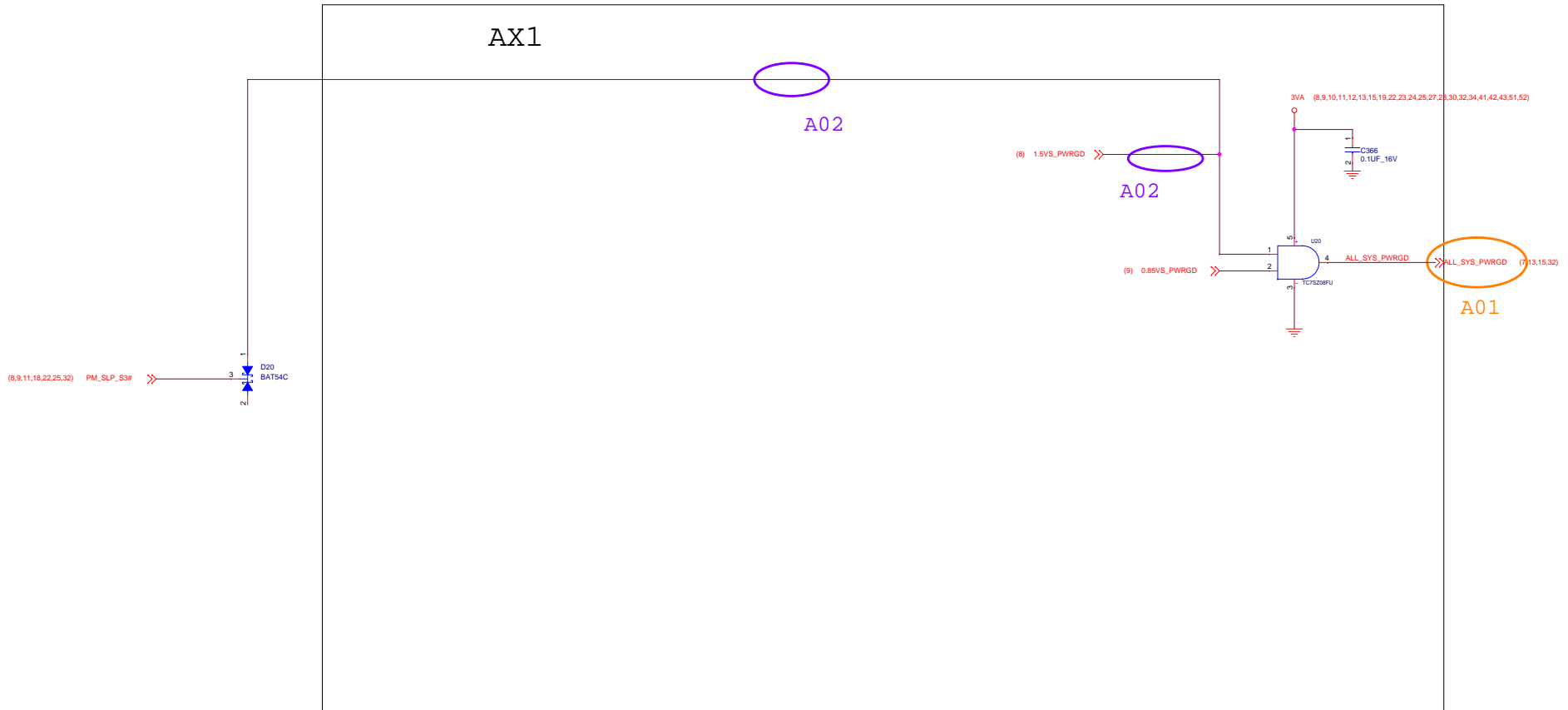
SCREW



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| INVENTEC | | | |
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| SIZE: C | CODE: CS | DOCNUMBER: CS-131 | REV: A02 |
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POWER SEQUENCE

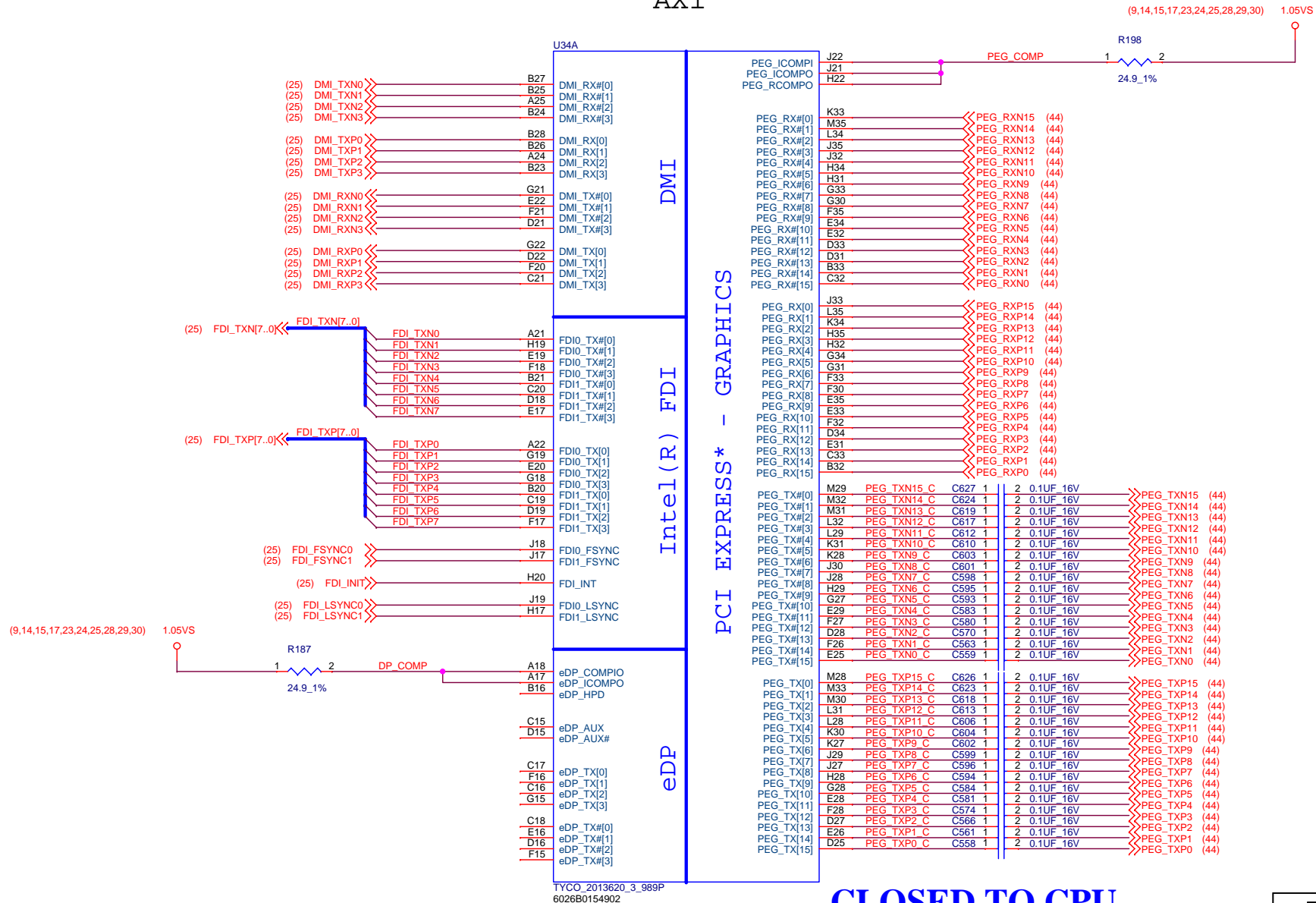


AX1
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| | | | |
|-----------------|-------------|--------------------------|------------|
| INVENTEC | | | |
| TITLE | | Strike POWER SEQUENCE | |
| SIZE Custom | CODE A03 | DOC. NUMBER | REV A02 |
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Processor_DMI,FDI,PCI_e

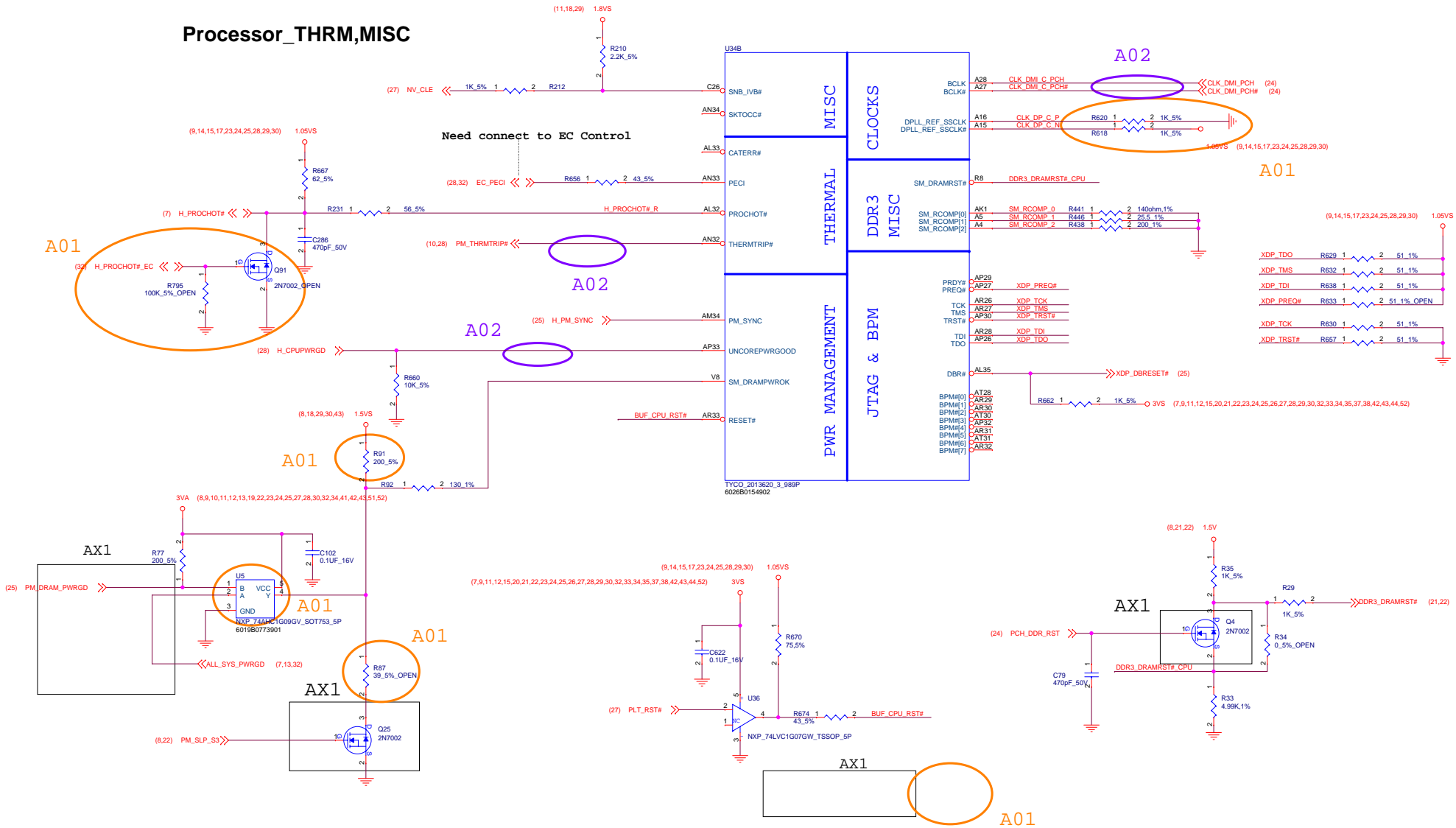
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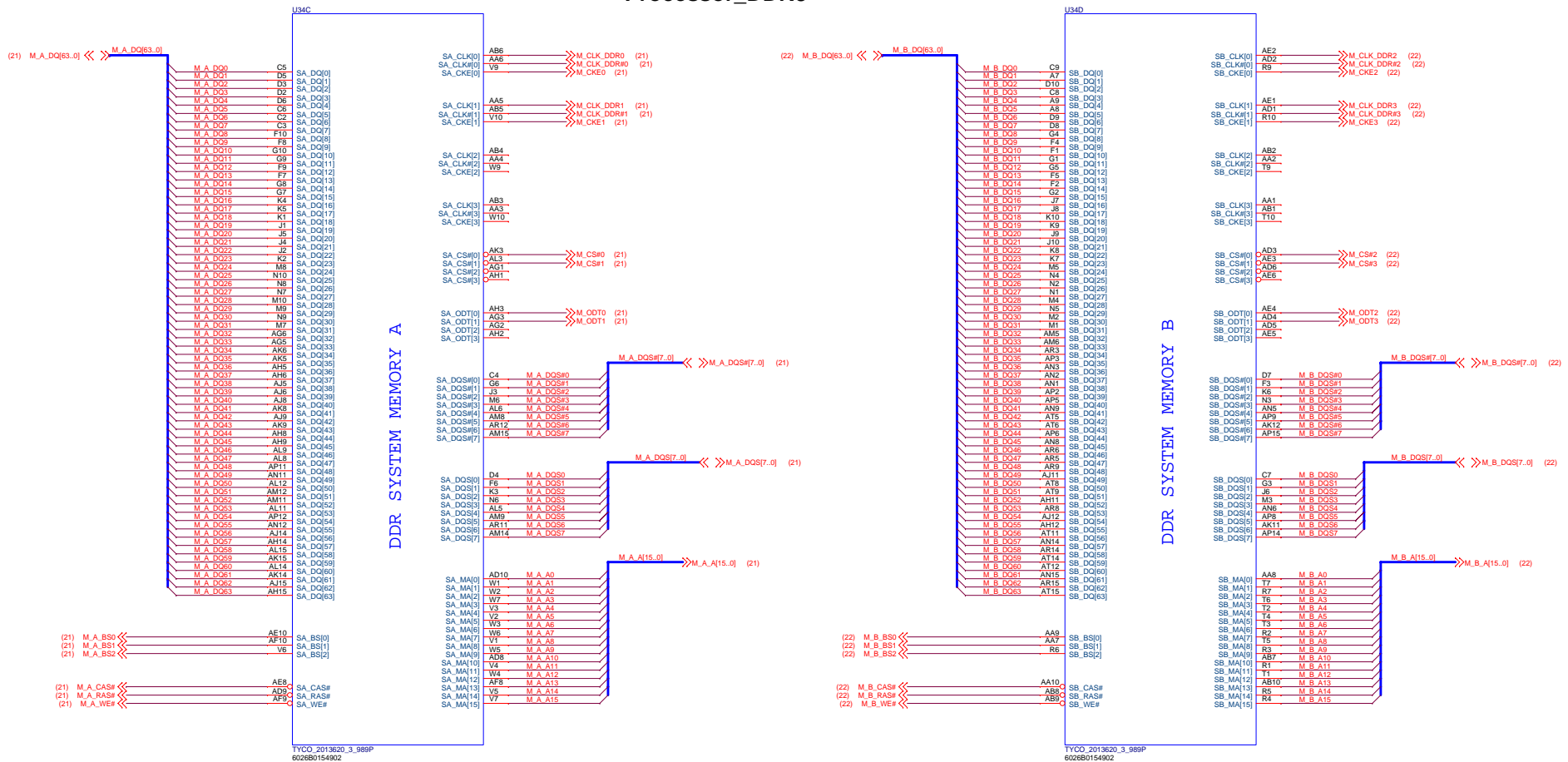
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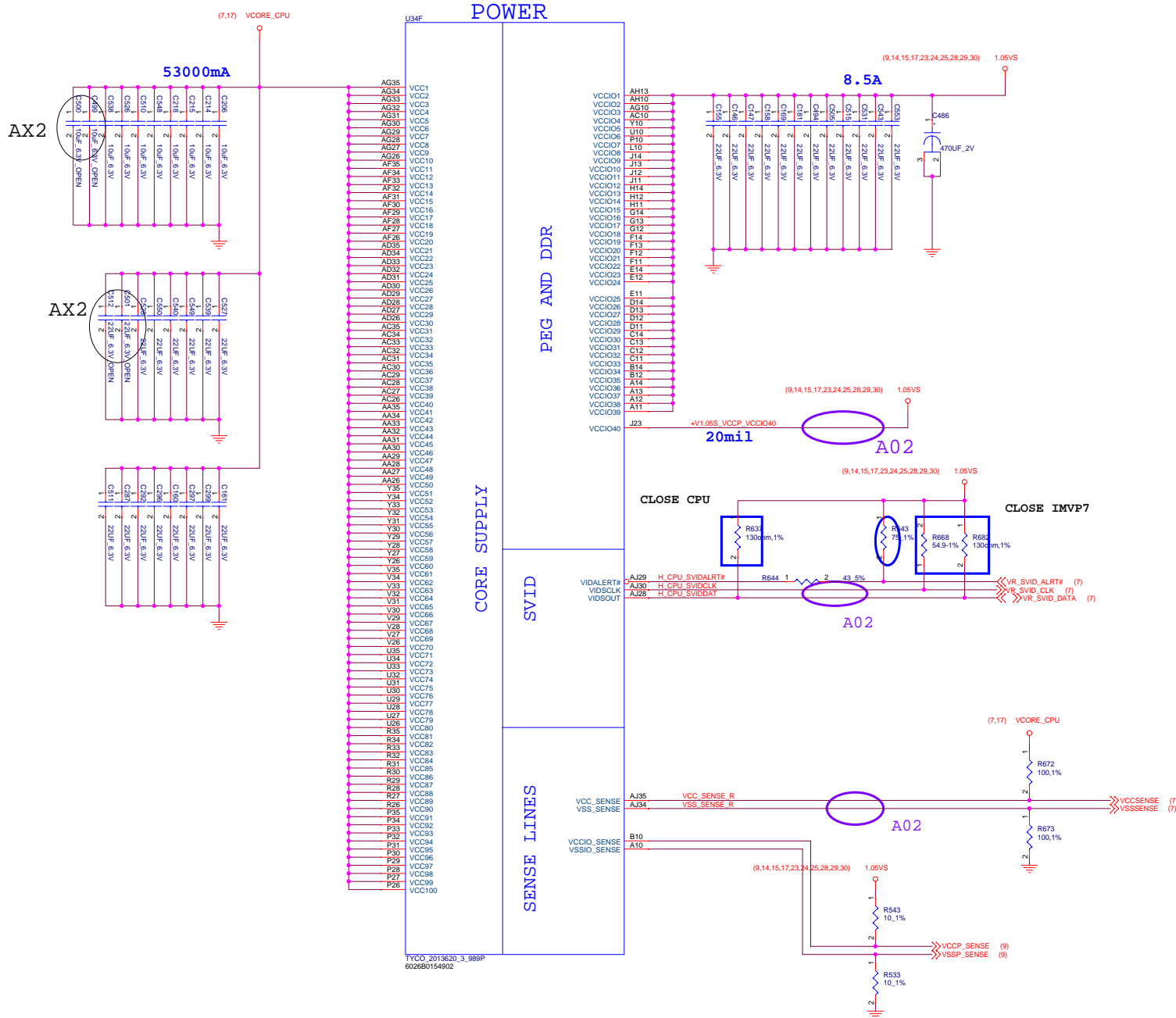
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|-----------------------|------|------------|-------|--|
| TITLE | | | | |
| Strike Processor(1/6) | | | | |
| SIZE | CODE | DOC.NUMBER | REV | |
| B | CS | CS-131 | A02 | |
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Processor_THRM,MISC



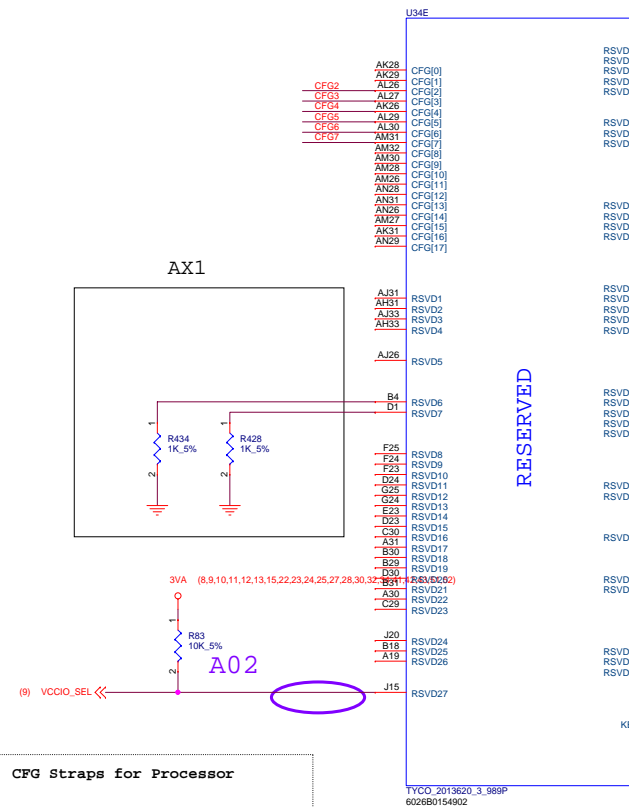
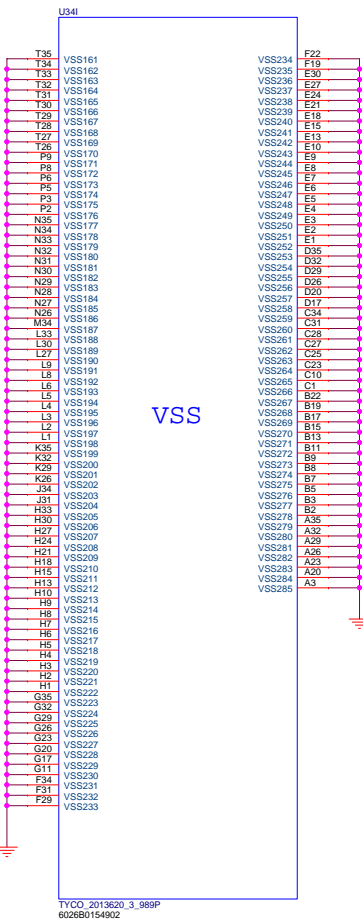
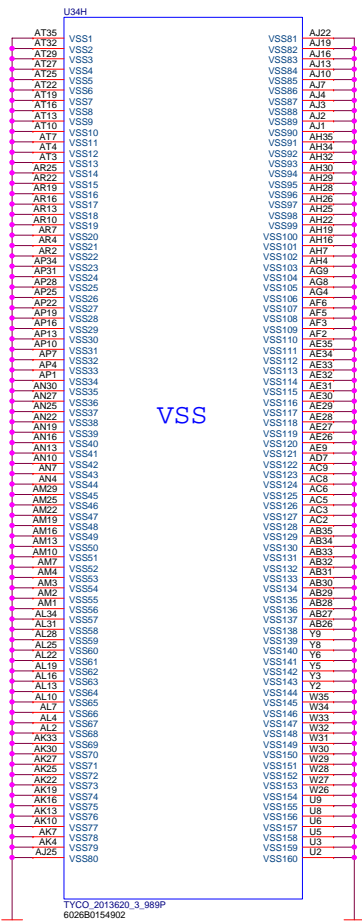
Processor_DDR3





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|------------------------------|----------|-------------------|----------|
| TITLE: Strike Processor(4/6) | | | |
| SIZE: C | CODE: CS | DOC NUMBER: CS-13 | REV: A02 |
| SHEET | | 17 | of 55 |



PEG Static Lane Reversal - CFG2 is for the 16x

CFG2 1:(Default) Normal Operation; Line # definition matches socket pin map definition
0:Lane Reversed

Display Port Presence Strap

CFG2 1:(Default) Normal Operation; Line # definition matches socket pin map definition
0:Lane Reversed

PCIe Port Bifurcation Straps

CFG[6:5] 11:(Default)x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING

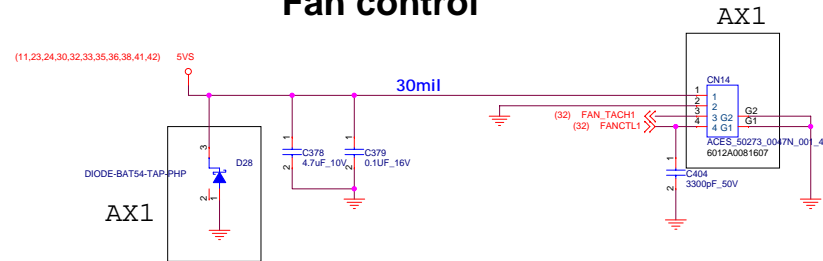
CFG7 1:(Default) PEG Train immediately following RESETB de assertion
0:PEG Wait for BIOS for training

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| Strike Processor(6/6) | | | |
|-----------------------|------|------------|-------|
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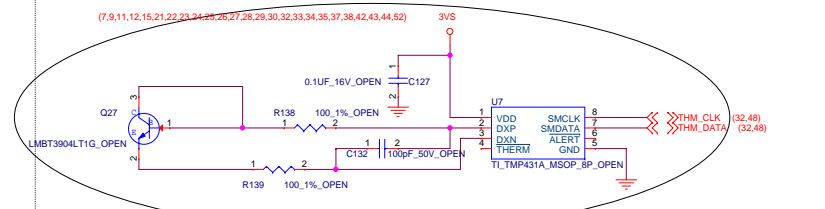
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Fan control



GPU Thermal sensor

REMOTE thermal sensor
Place near the hottest spot area under Palm-rest



AX2

AX2

A02

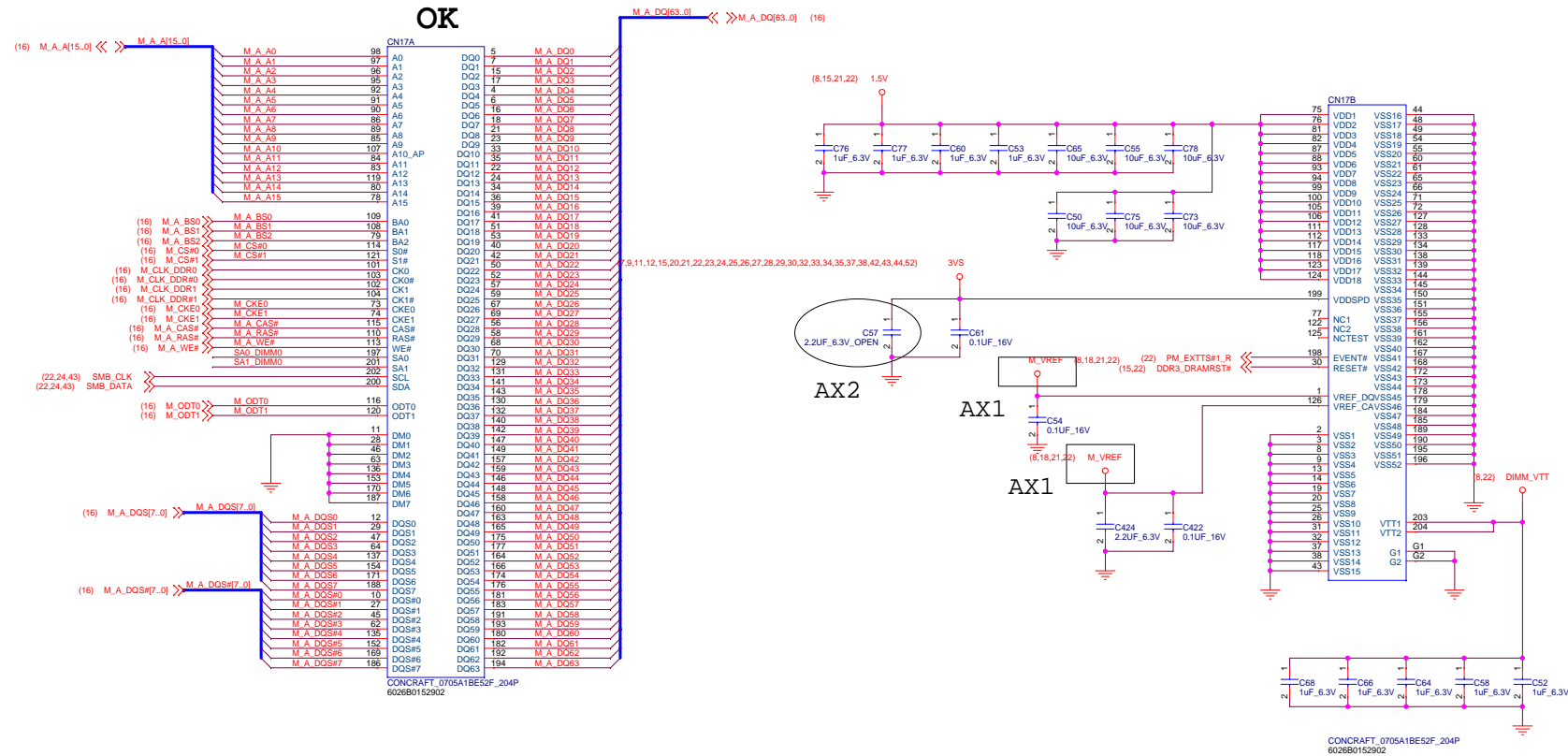
A02

→ THRM_SD# (10,48)

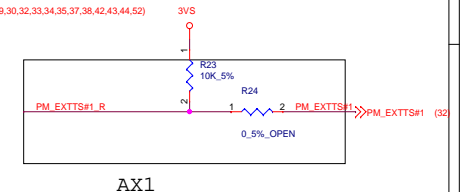
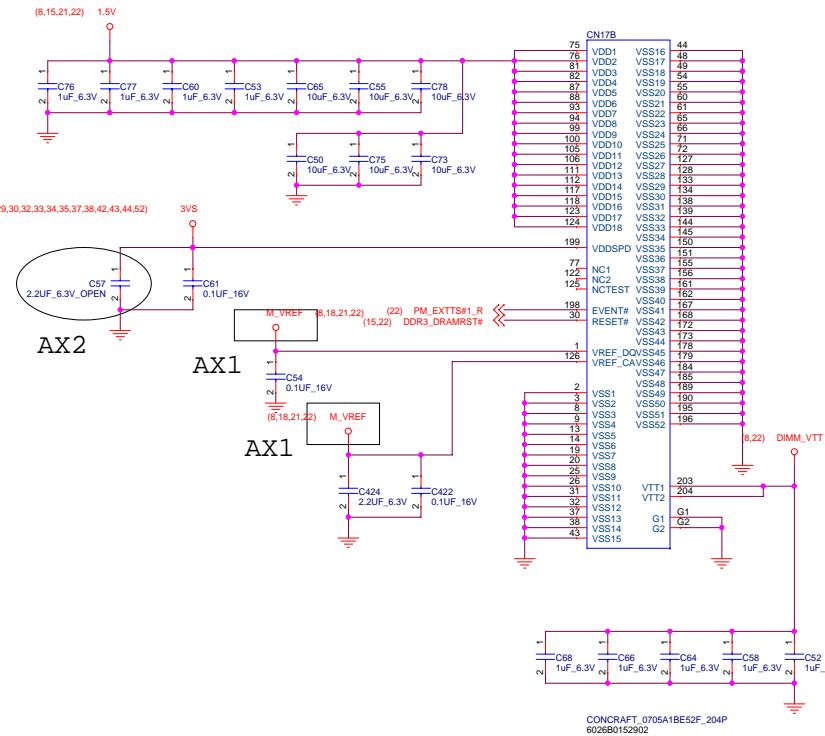
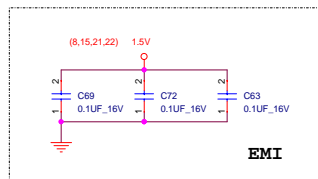
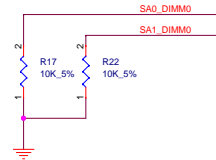
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| | | | |
|-----------------------|------------|-----------------------|------------|
| TITLE | | | |
| Strike Fan/Thermal | | | |
| SIZE C | CODE CS | DOC. NUMBER CS-131 | REV A02 |
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SO-DIMMO



NOTE:
IF SA0_DIMMO=0, SA1_DIMMO=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30
IF SA0_DIMMO=1, SA1_DIMMO=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32

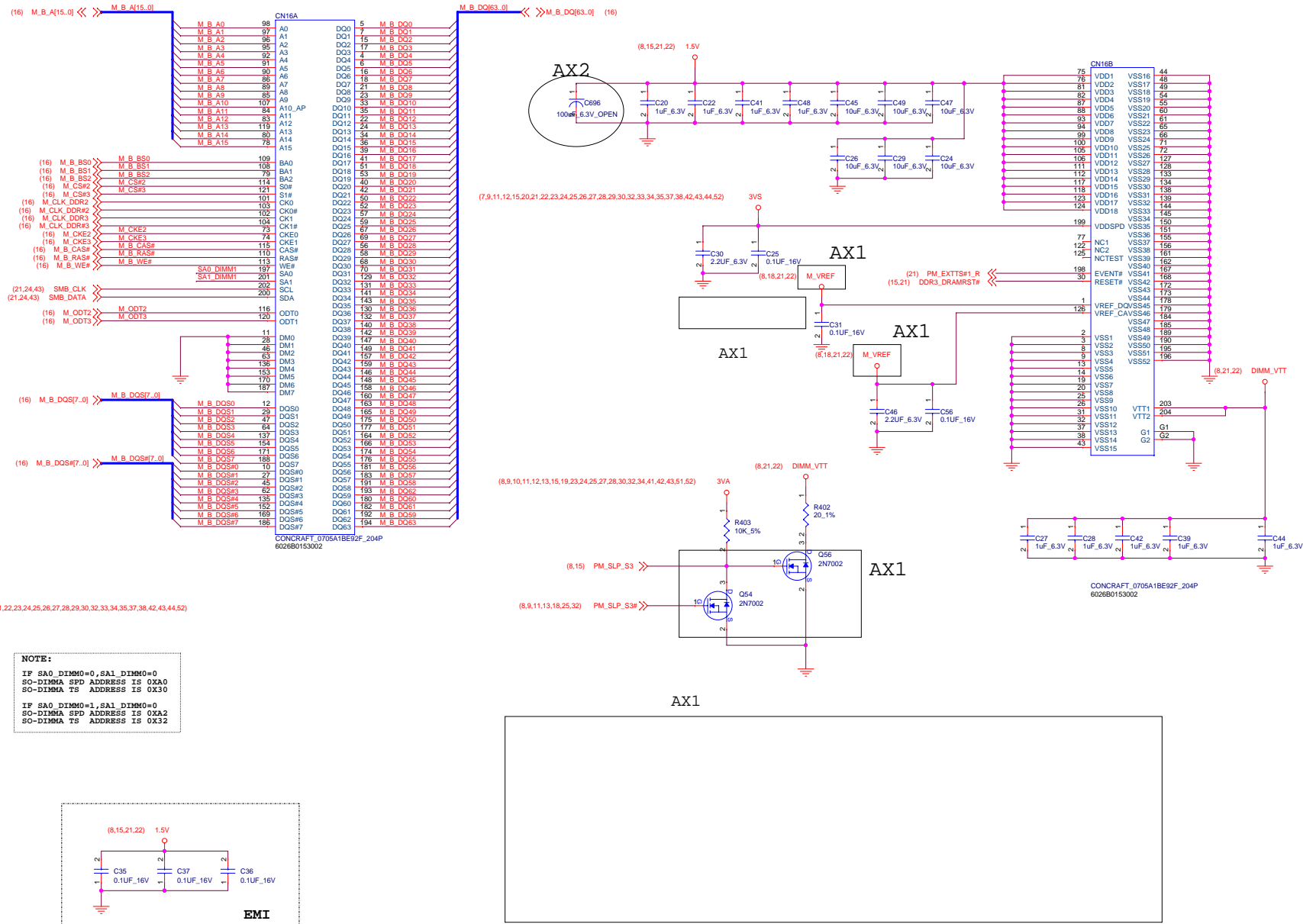


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| INVENTEC | | | |
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| Strike | | | |
| DDR3 SDRAM SO-DIMM 1/2 | | | |
| SIZE | CODE | DOC. NUMBER | REV |
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SO-DIMM1

OK



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INVENTEC

| TITLE | | | |
|-----------------------|------|------------|-----|
| Strike | | | |
| DDR3 SDRAM SO-DIMM 22 | | | |
| SIZE | CODE | DOC NUMBER | REV |
| C | CS | CS-131 | A02 |
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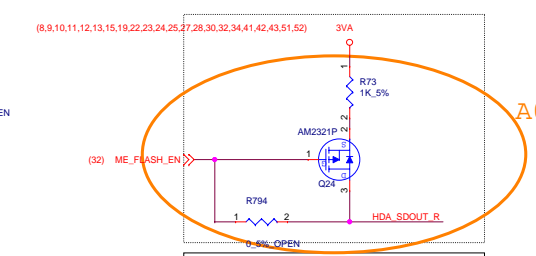
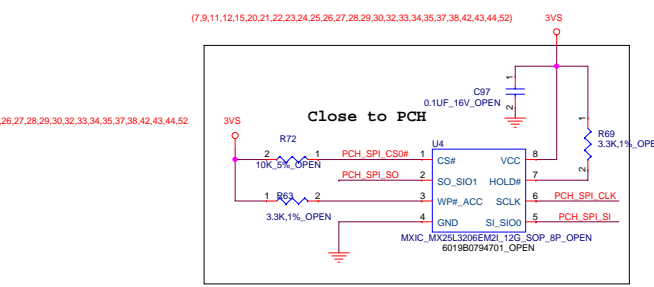
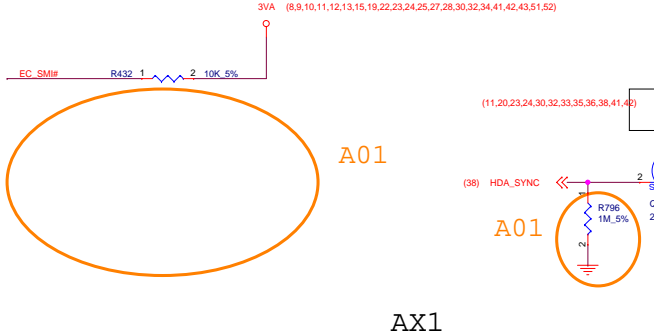
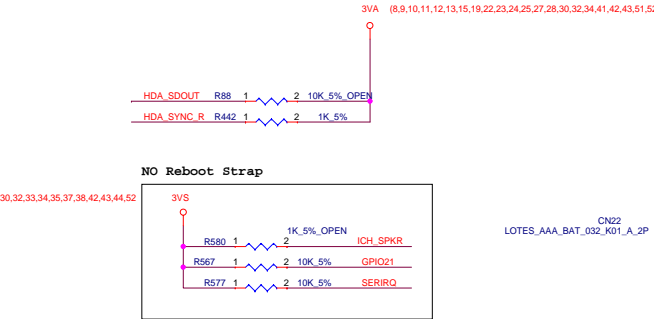
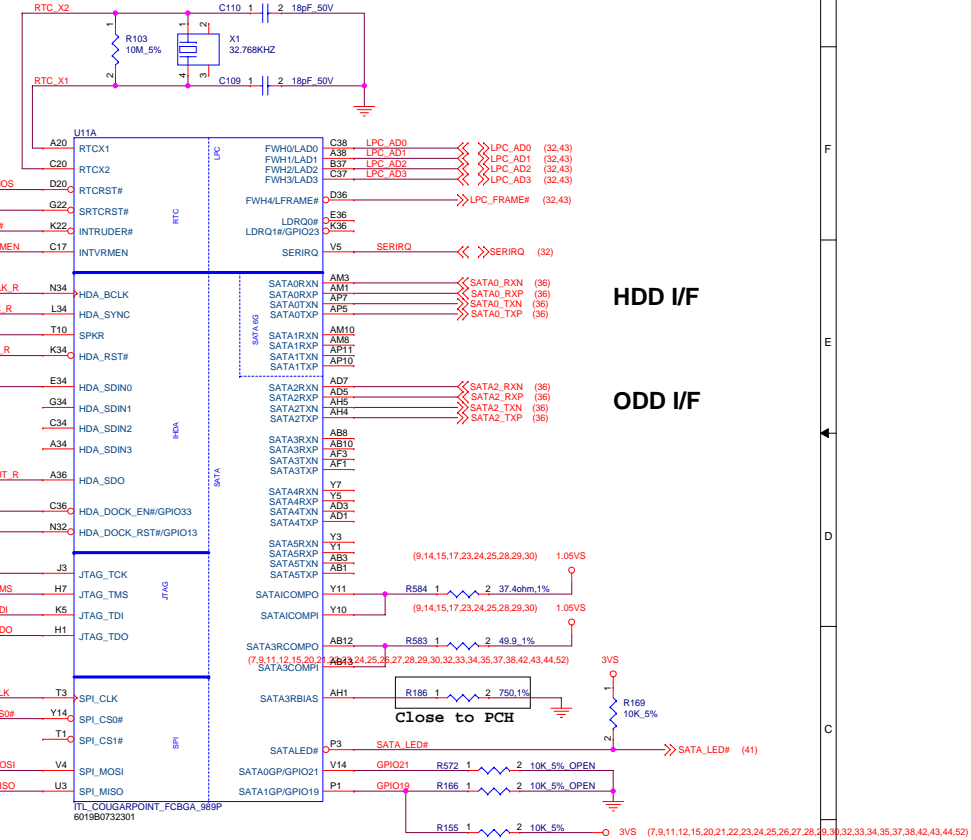
CHANGE by IEC DATE Friday, December 17, 2010

located on DIMM window area.

CL1 CL2

J1

JUMP2_200_32

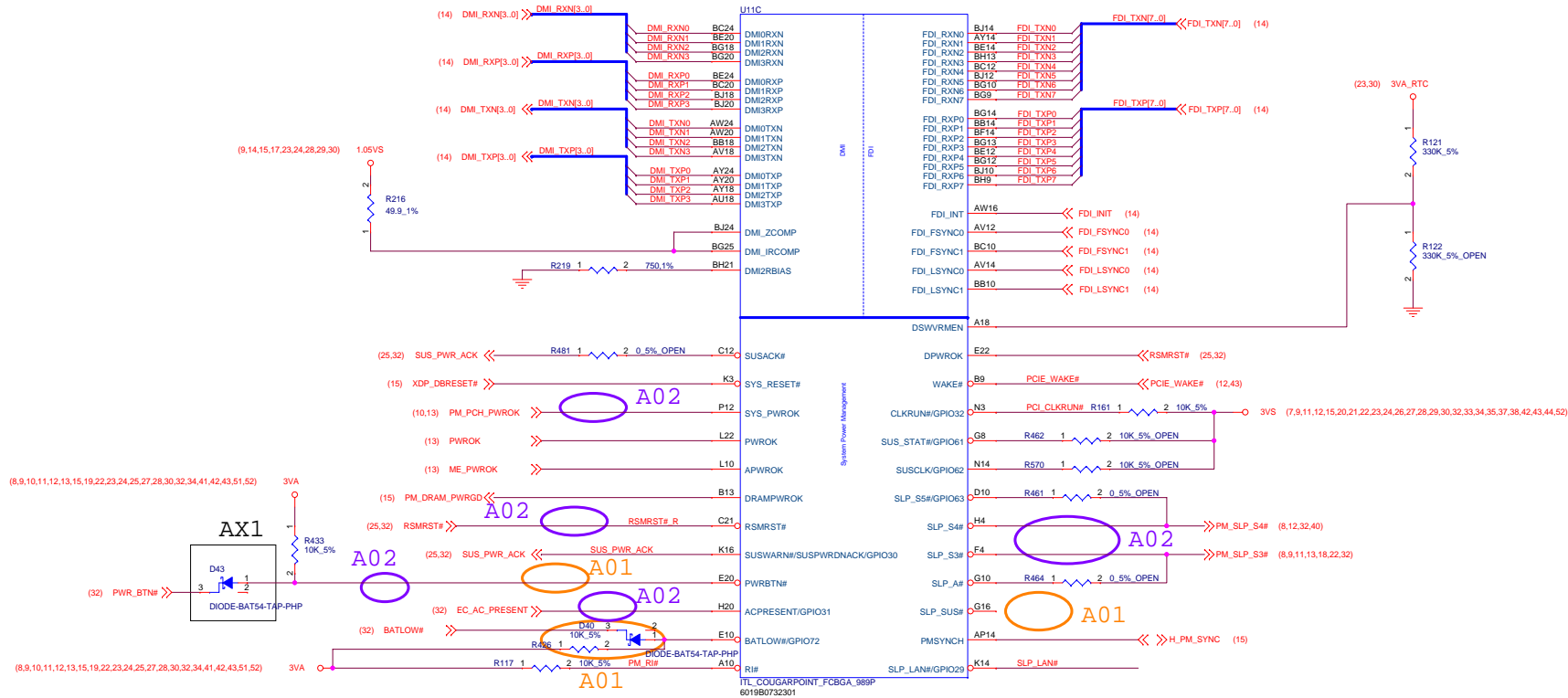
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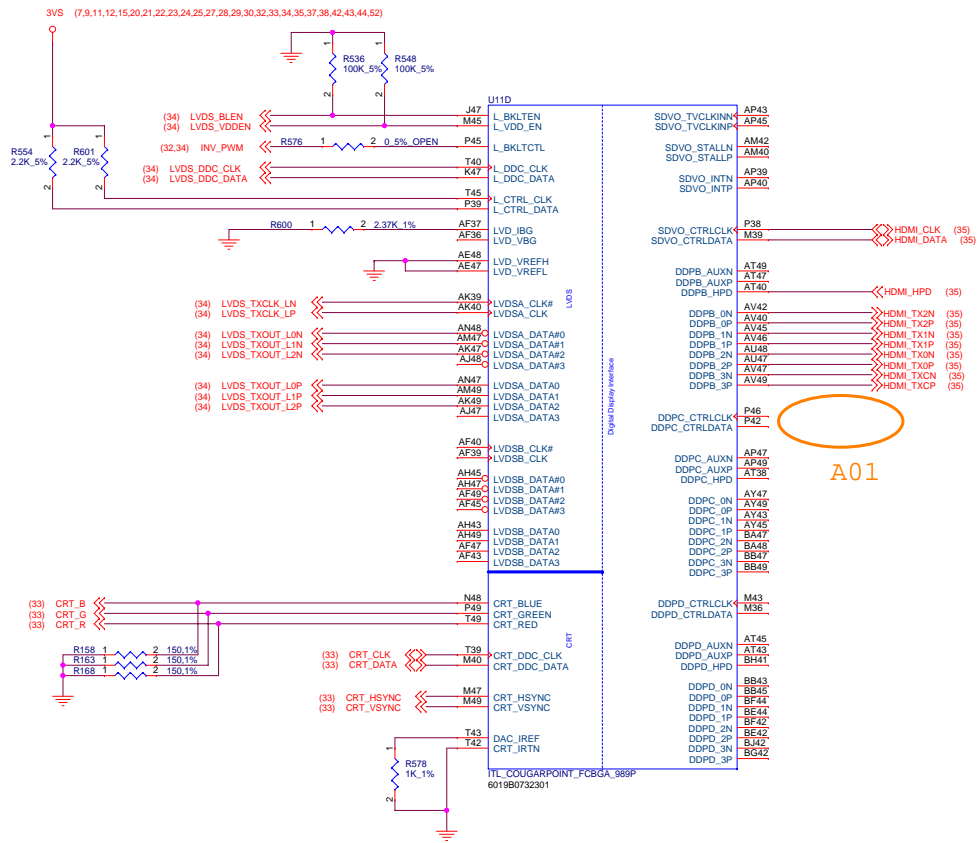
| Flash Descriptor Security Override | |
|------------------------------------|---------------|
| HDA_SDOUT_R | High : Enable |
| | Low : Disable |

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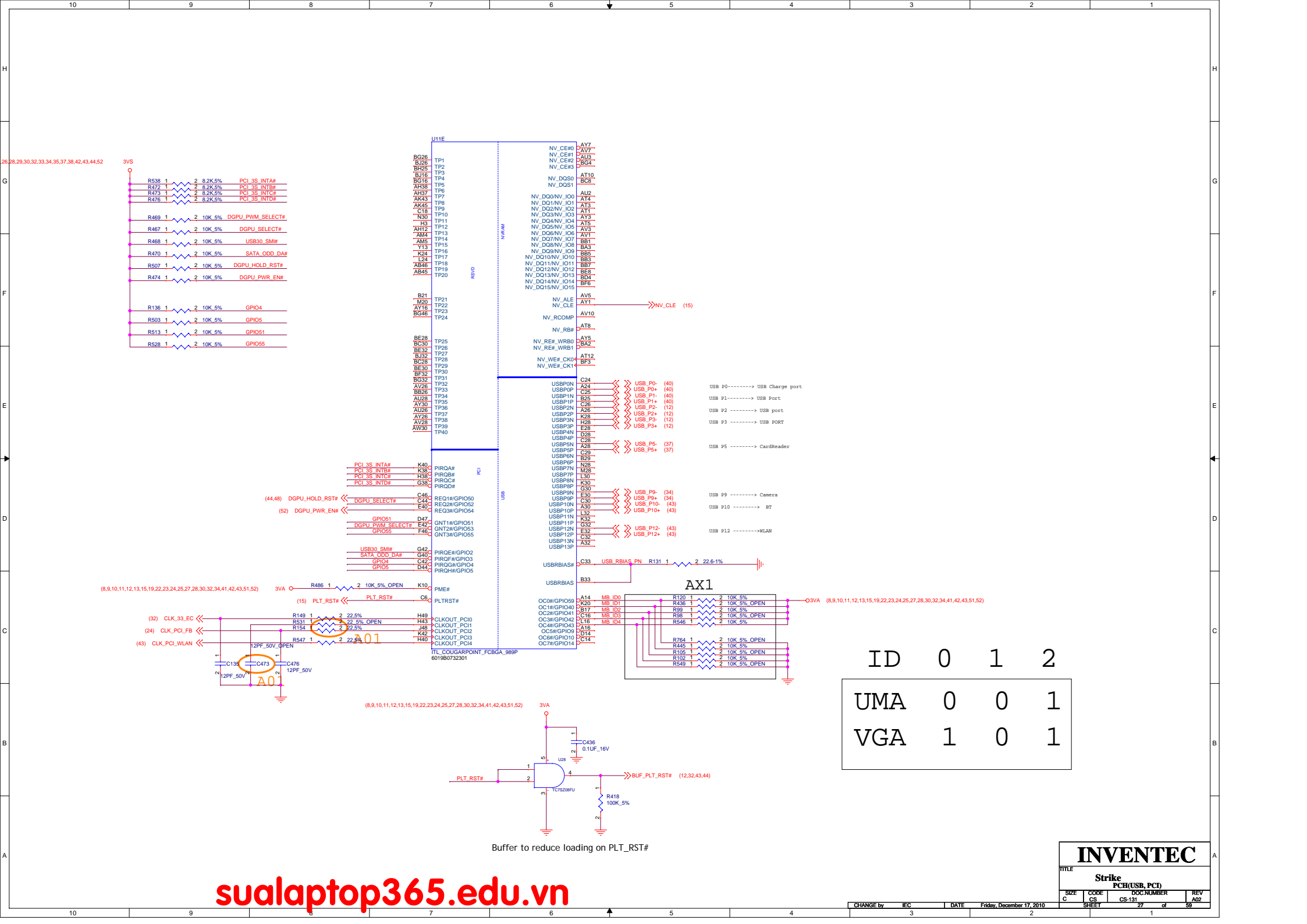
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|-----------------------------|------------|----------------------|------------|
| TITLE | | | |
| Strike PCH(SATA,RTC,SPI) | | | |
| SIZE C | CODE CS | DOC.NUMBER CS-131 | REV A02 |
| SHEET | | 23 | of 59 |

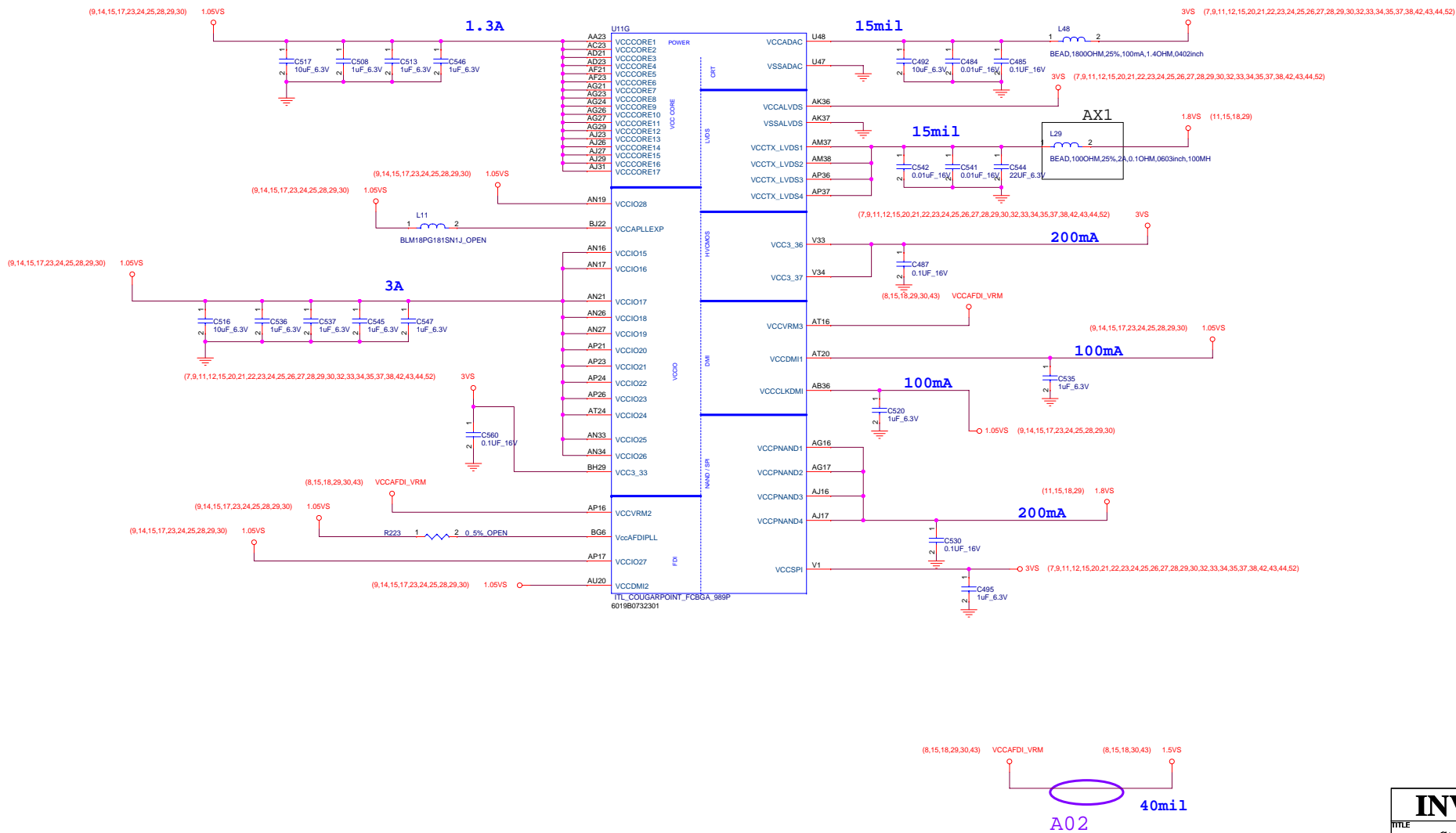


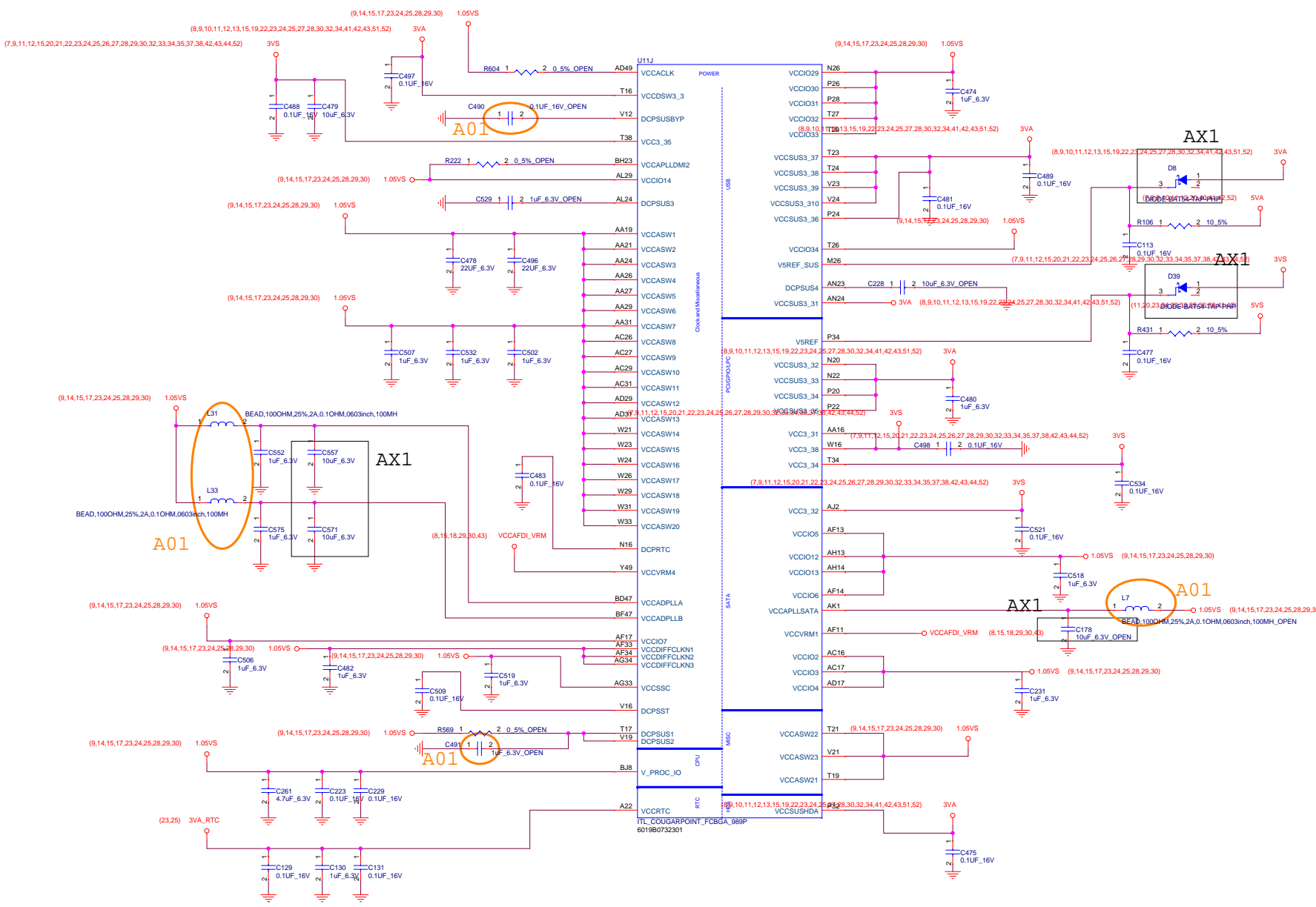


A01

Place 150ohm termination resistor close to GMCH

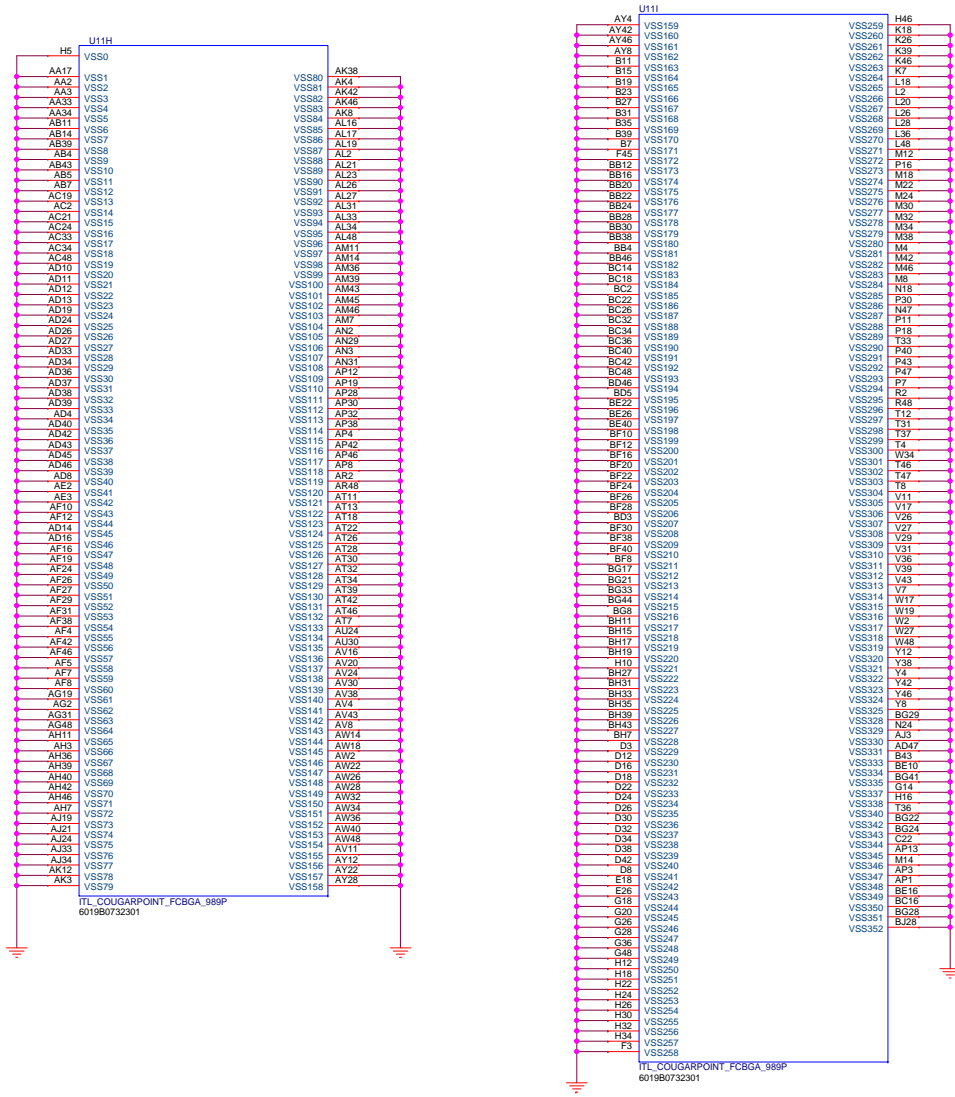




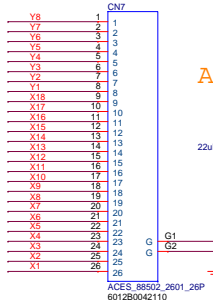
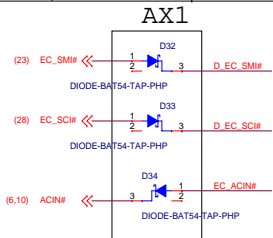


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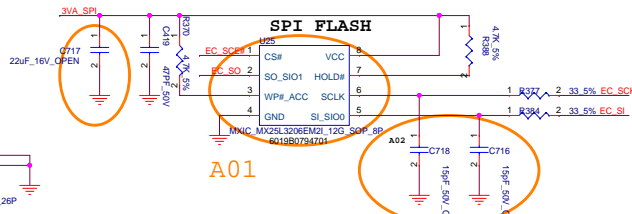
| INVENTEC | | | |
|---------------------------|----------|--------------------|----------|
| TITLE: Strike PCH Power 2 | | | |
| SIZE: C | CODE: CS | DWG NUMBER: CS-131 | REV: A02 |
| SHEET | | 30 | of 59 |



| | VGA | UMA |
|------|---------|---------|
| R762 | Enable | Disable |
| R763 | Disable | Enable |

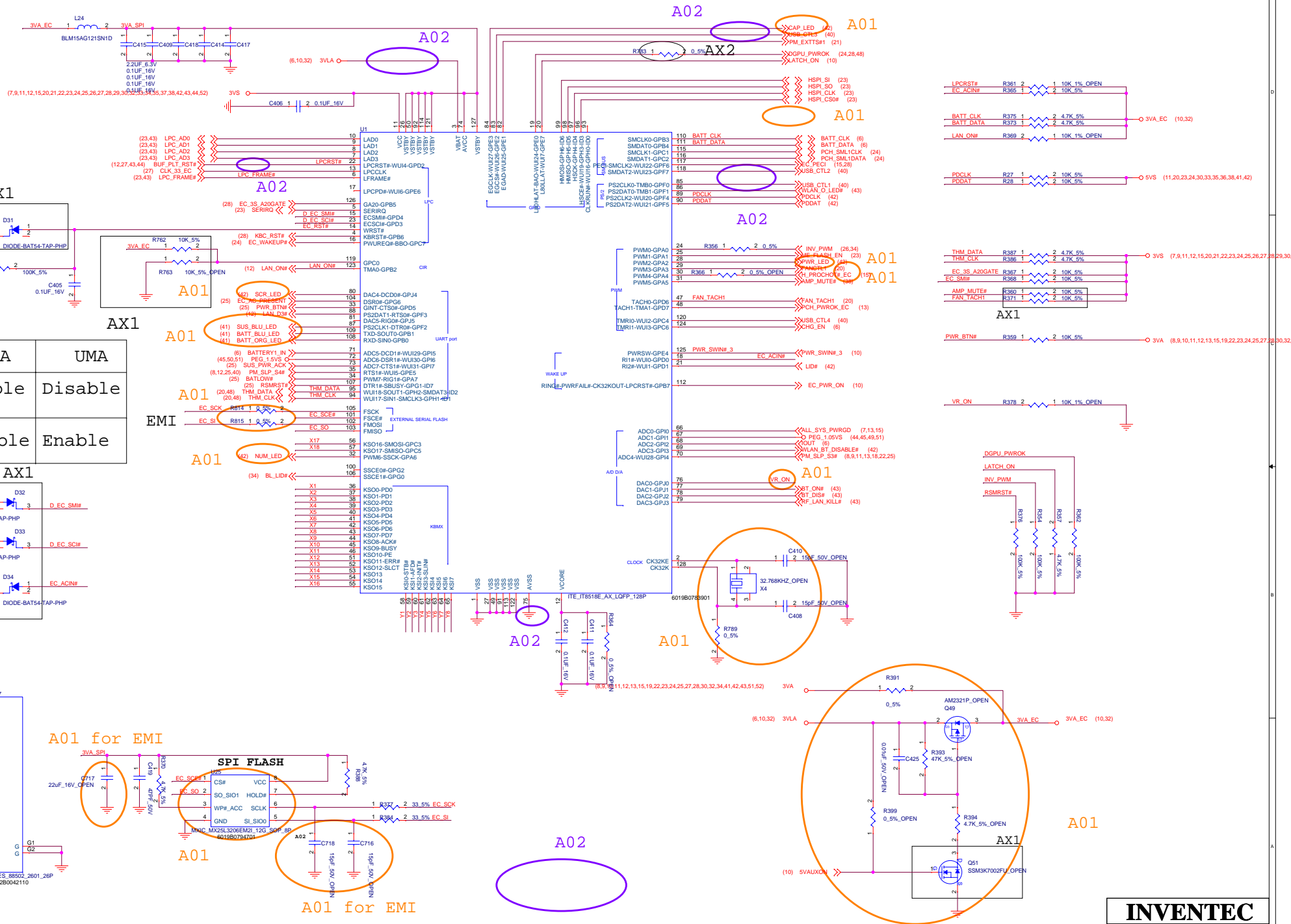


A01 for EMI



A01 for EMI

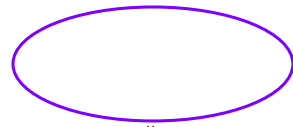
sualaptop365.edu.vn



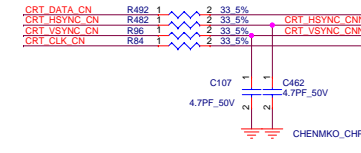
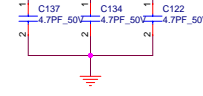
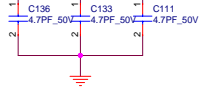
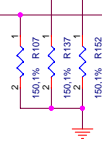
| INVENTEC | | | |
|---------------|----------|-------------------|---------|
| TITLE: Strike | | | |
| KBC | | | |
| SIZE: Custom | CODE: CS | DOCNUMBER: CS-131 | REV: 02 |
| SHEET | | 32 | of 39 |

CRT

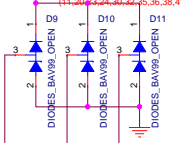
A02



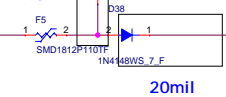
(26) CRT_R
(26) CRT_G
(26) CRT_B



20mil



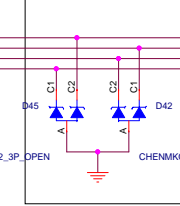
40mil



20mil



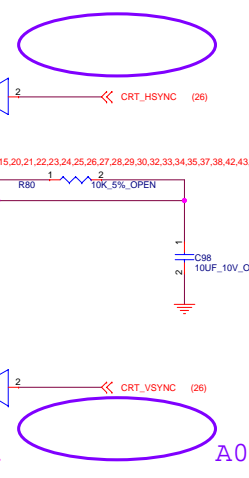
AX1



CRT CON.

AX1

A02



20mil

CRT_HSYNC_CN

U10

TC7SZ126FU_OPEN

CRT_HSYNC (26)

3VS

R80

10K, 5%, OPEN

C98

10UF, 10V, OPEN

CRT_VSYNC_CN

U6

TC7SZ126FU_OPEN

CRT_VSYNC (26)

AX1

R159

0.5%

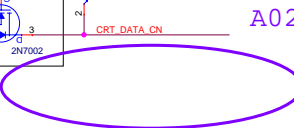
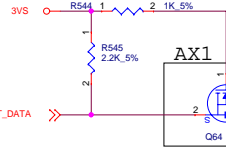
CRT_HSYNC

R89

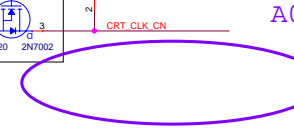
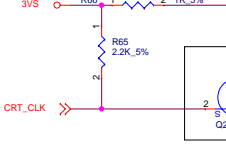
0.5%

CRT_VSYNC

(7,9,11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52)



(7,9,11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52)



INVENTEC

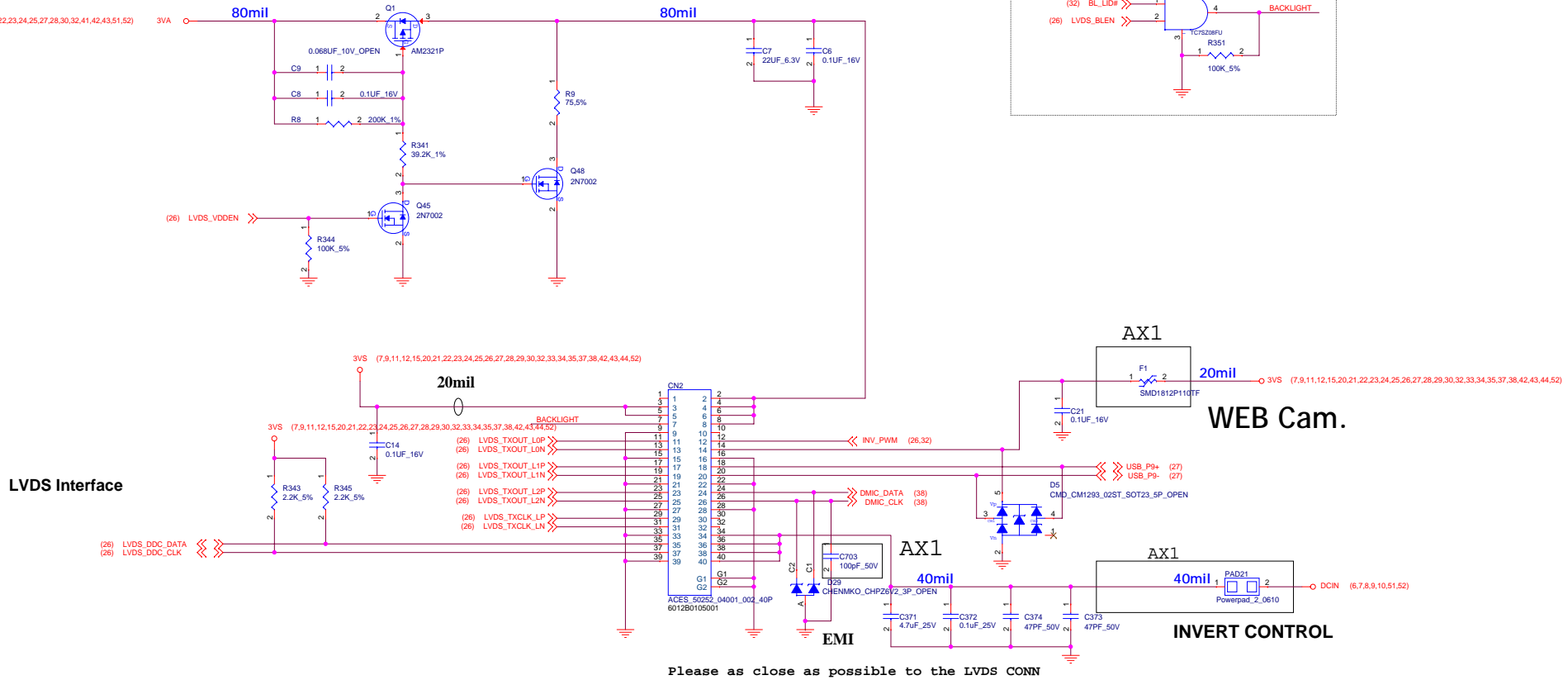
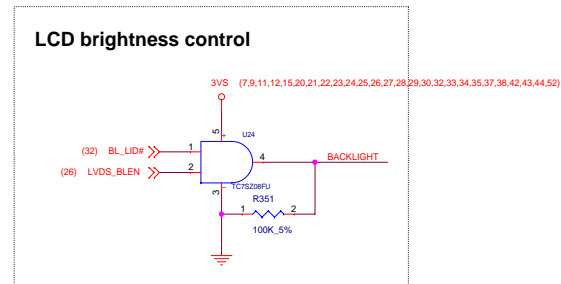
Strike CRT CNN

SIZE CODE DOC NUMBER REV
C CS CS-13 33 of 59

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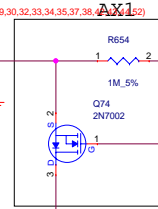
CHANGE by IEC DATE Friday, December 17, 2010

SHEET



Please as close as possible to the LVDS CONN

(7,9,11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,44,52)



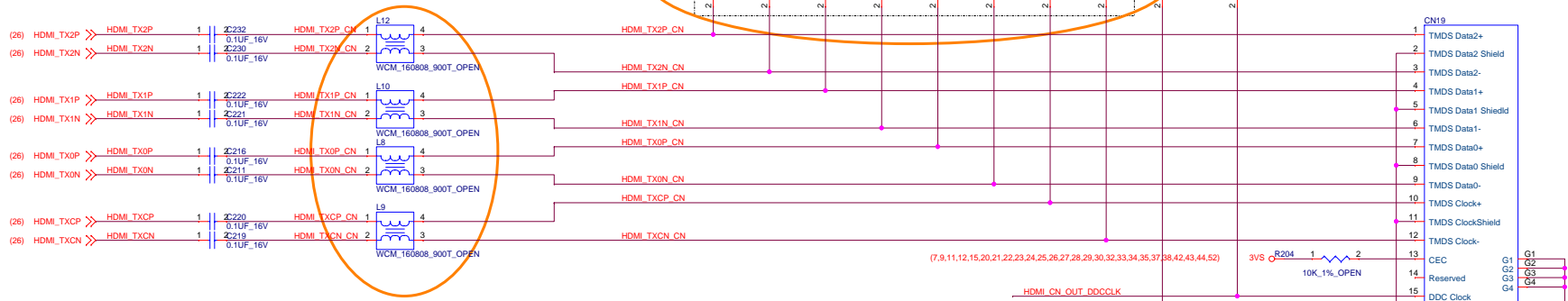
HDMI CONN

(11,20,23,24,30,32,33,35,36,38,41,42)

5V5
D46
DIODE-BAT54-TAP-PHP

A01

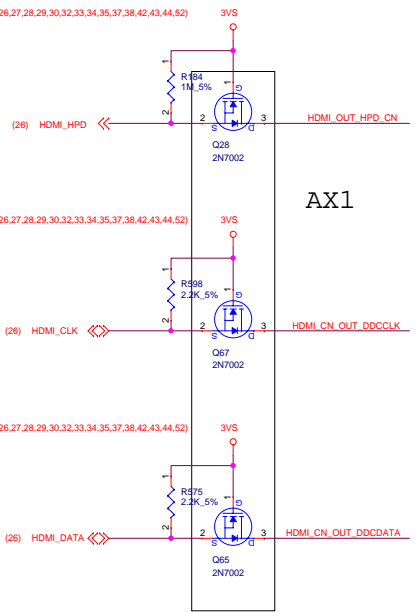
A01 for EMI



AX1

(33) 5V5_HDMI
20mil

(7,9,11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52)



AX1

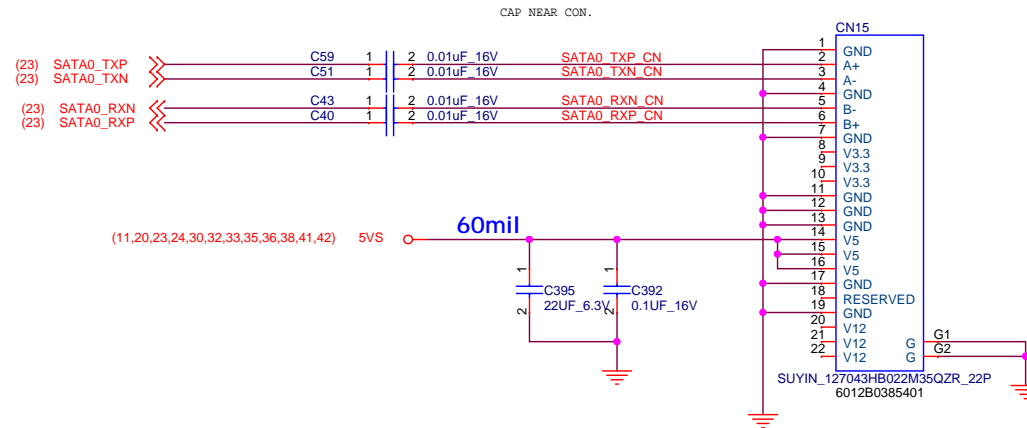
(7,9,11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52)

(7,9,11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52)

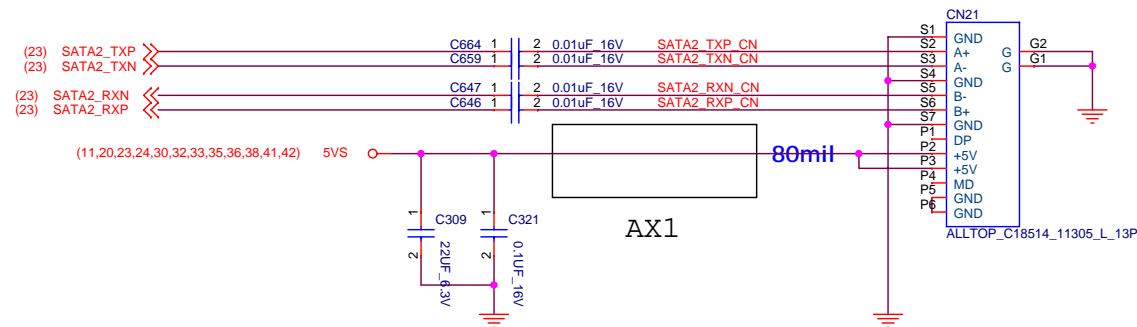
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| INVENTEC | | | |
|----------|------|------------|-----|
| TITLE | | | |
| Strike | | | |
| HDMI CNN | | | |
| SIZE | CODE | DOC NUMBER | REV |
| C | CS | CS-13 | A02 |
| SHEET | | | |
| 35 of 59 | | | |

HDD I/F



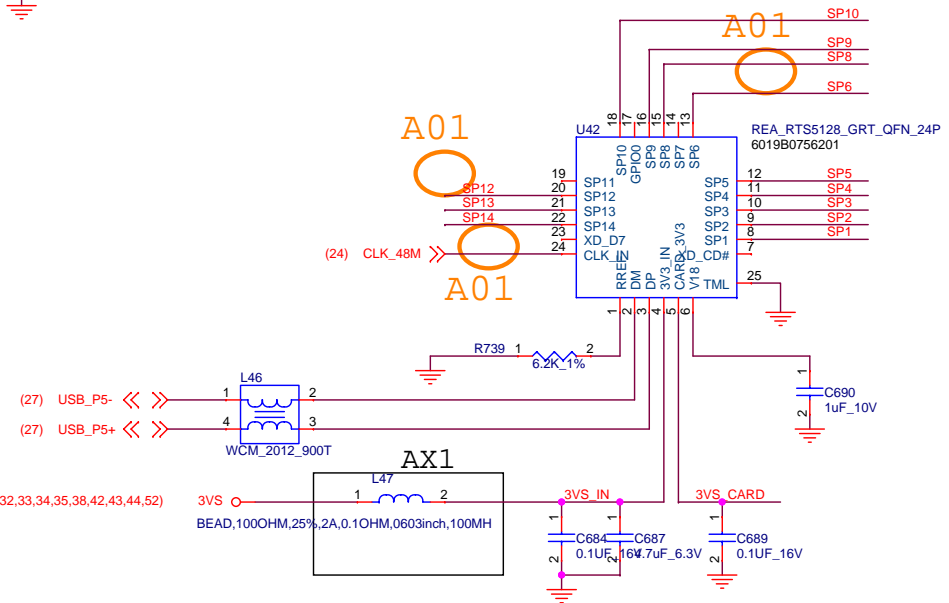
ODD I/F



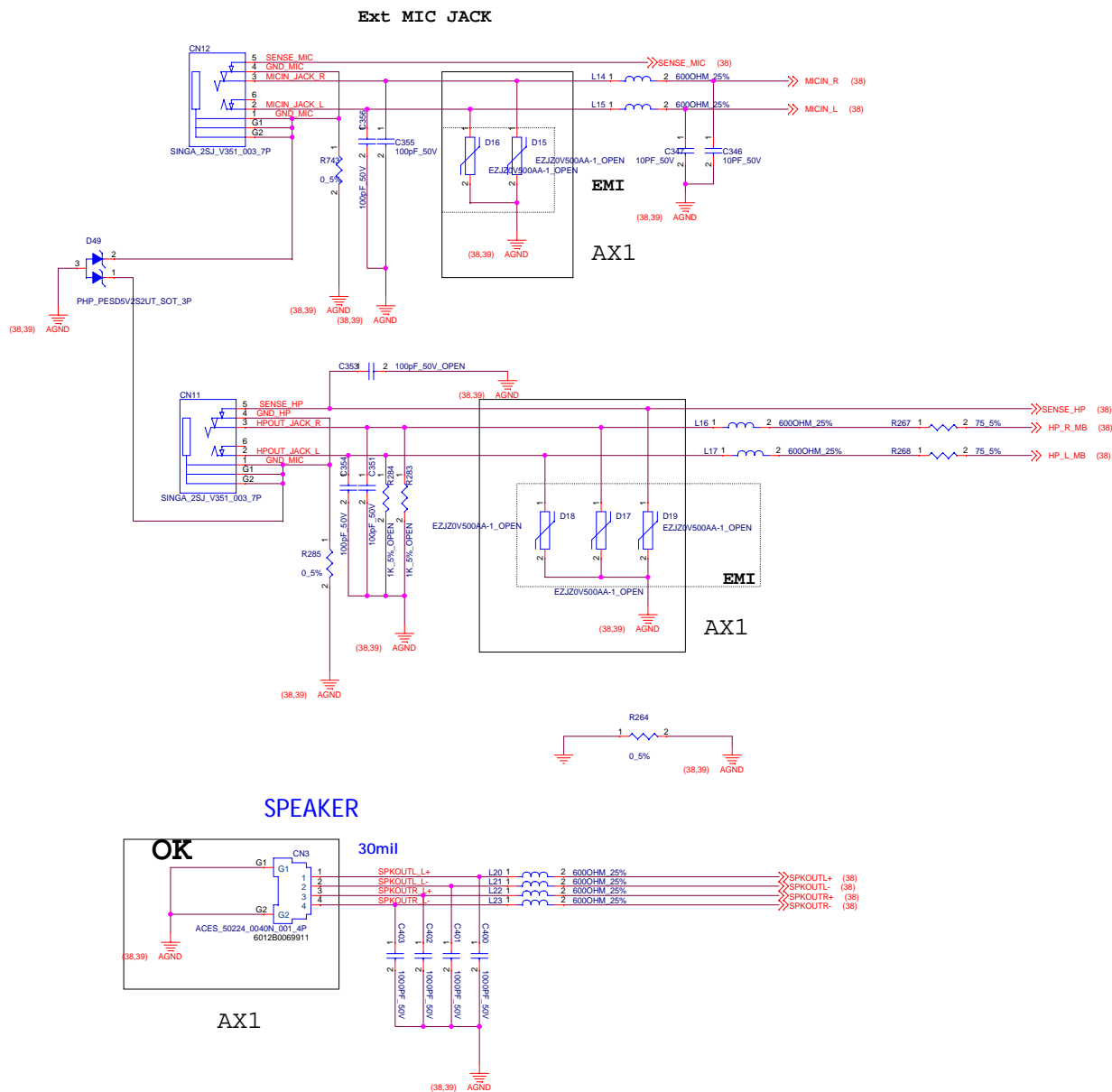
INVENTEC

| TITLE | | | |
|----------------|------|------------|-----|
| Strike HDD/ODD | | | |
| SIZE | CODE | DOC.NUMBER | REV |
| B | CS | CS-131 | A02 |
| SHEET | | 36 of 59 | |

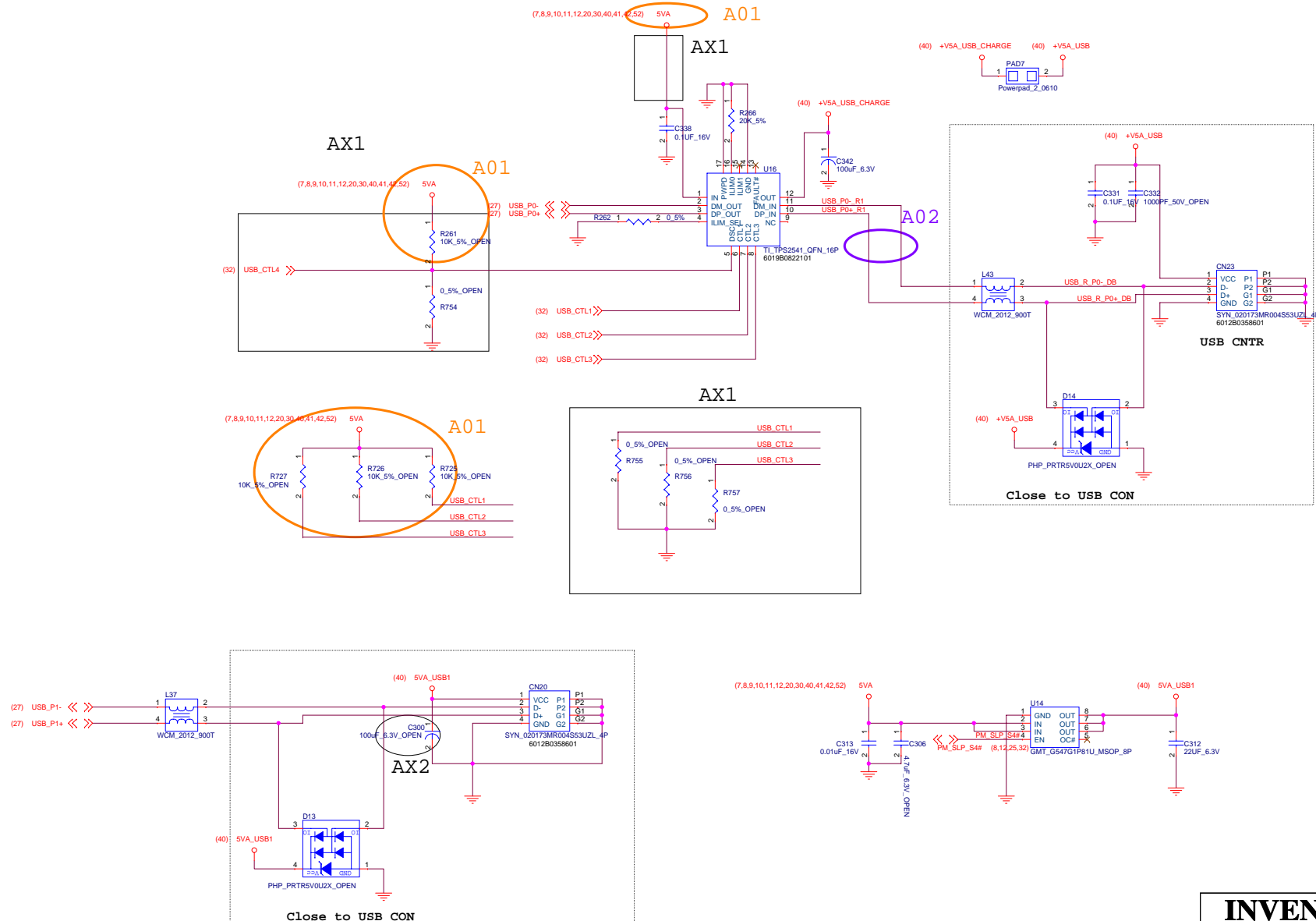
CHANGE by IEC DATE Friday, December 17, 2010



| | | | | | | | | |
|-----------|--|-----|------|---------------------------|----------------|----|--------|-----|
| CHANGE by | | IEC | DATE | Friday, December 17, 2010 | B | CS | CS-131 | A02 |
| | | | | | SHEET 37 of 59 | | | |



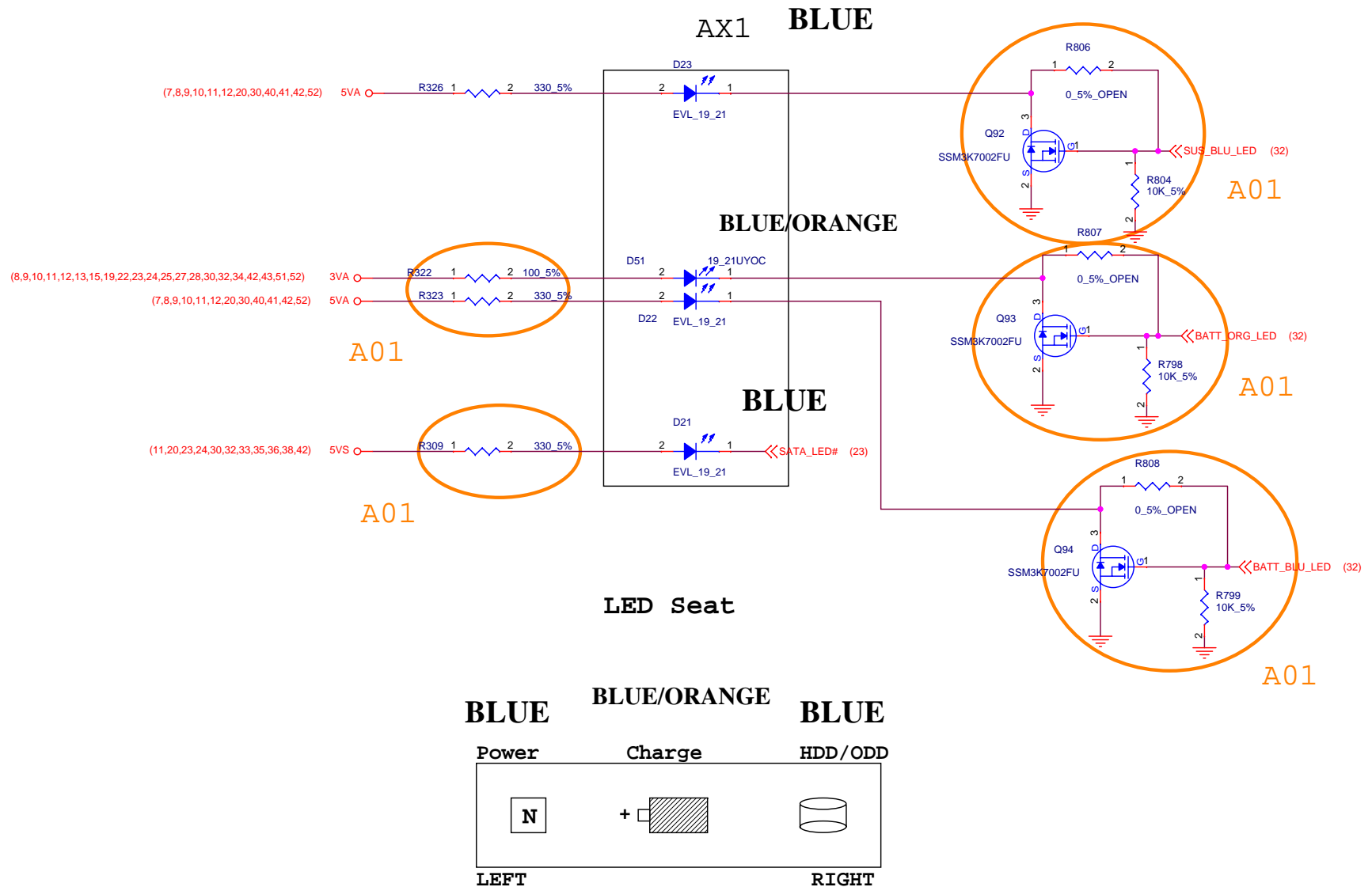
Power OFF Charge USB



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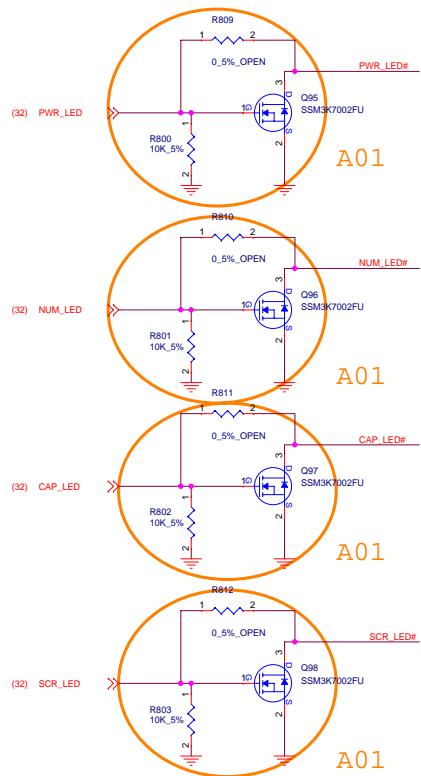
INVENTEC

| Strike Charge USB | | | |
|-------------------|------|-----------|-----|
| SIZE | CODE | DOCNUMBER | REV |
| C | CS | CS-131 | A02 |
| SHEET | 40 | of | 55 |

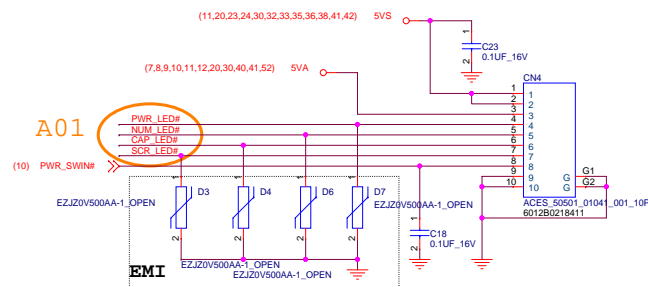


| INVENTEC | | | |
|-------------------------|---------|-------------------|---------|
| TITLE Strike LED | | | |
| SIZE B | CODE CS | DOC.NUMBER CS-131 | REV A02 |
| SHEET | 41 | of | 59 |

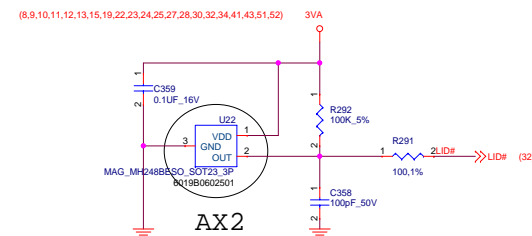
CHANGE by IEC DATE Friday, December 17, 2010



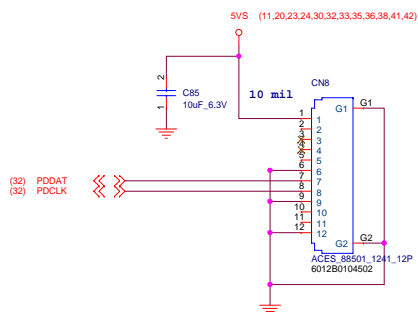
EMI POWER BUTTON BOARD



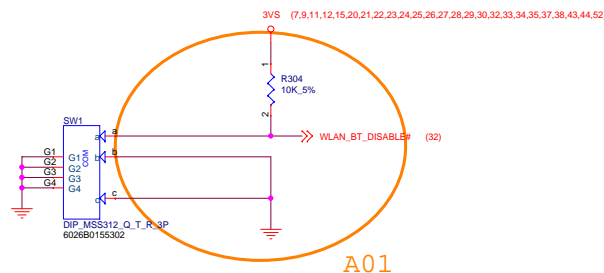
HALL Switch



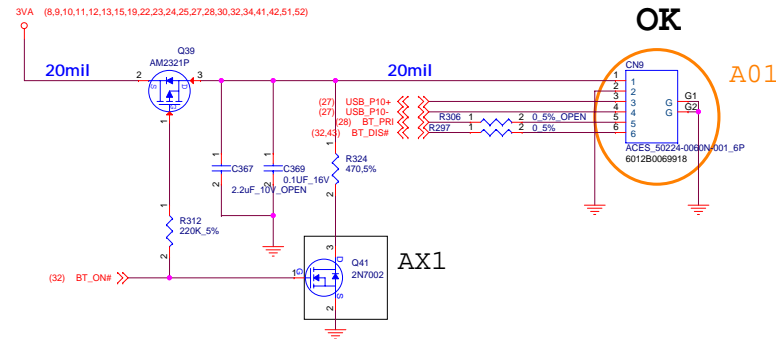
GP CNN.



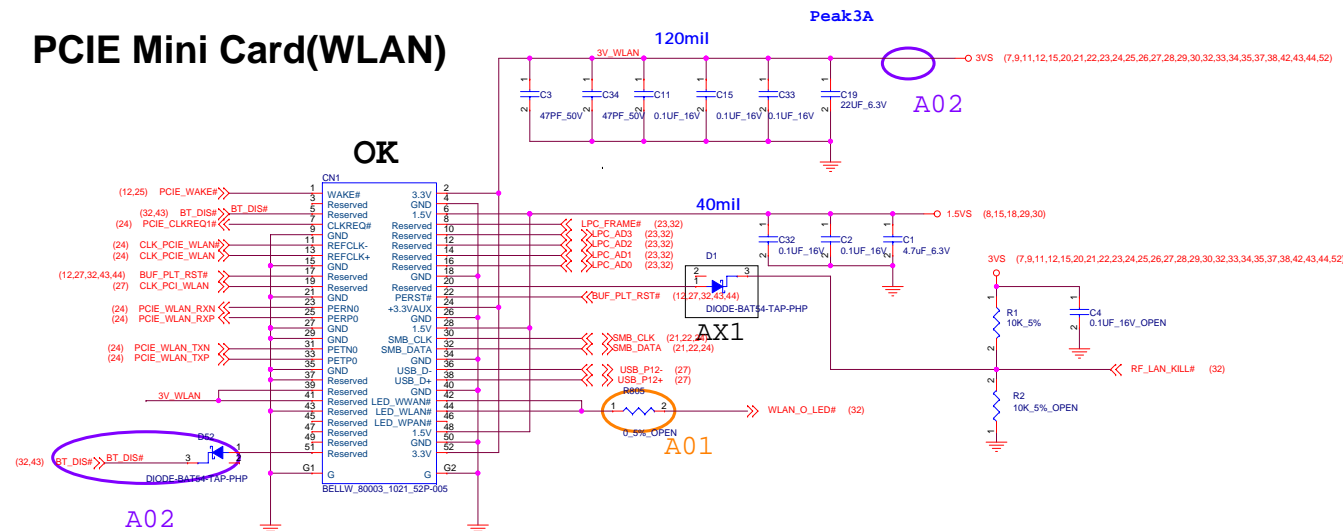
(W-LAN, BT) sliding switch



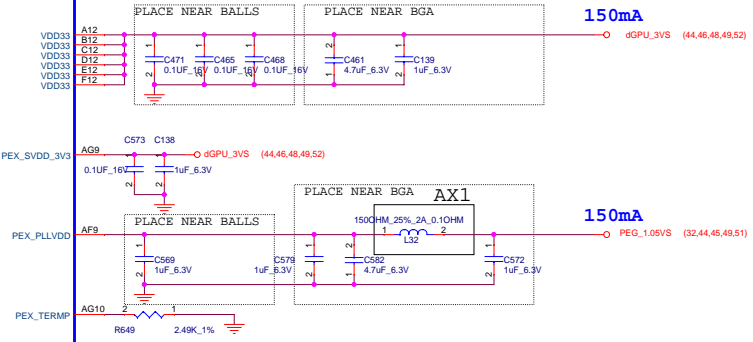
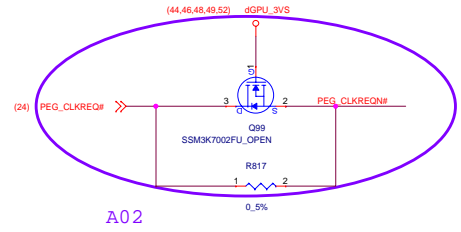
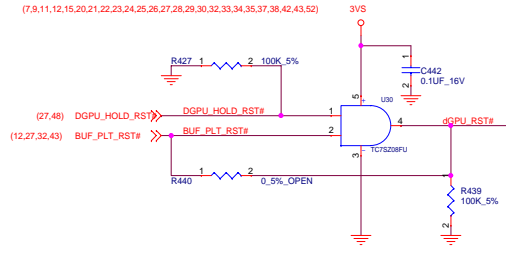
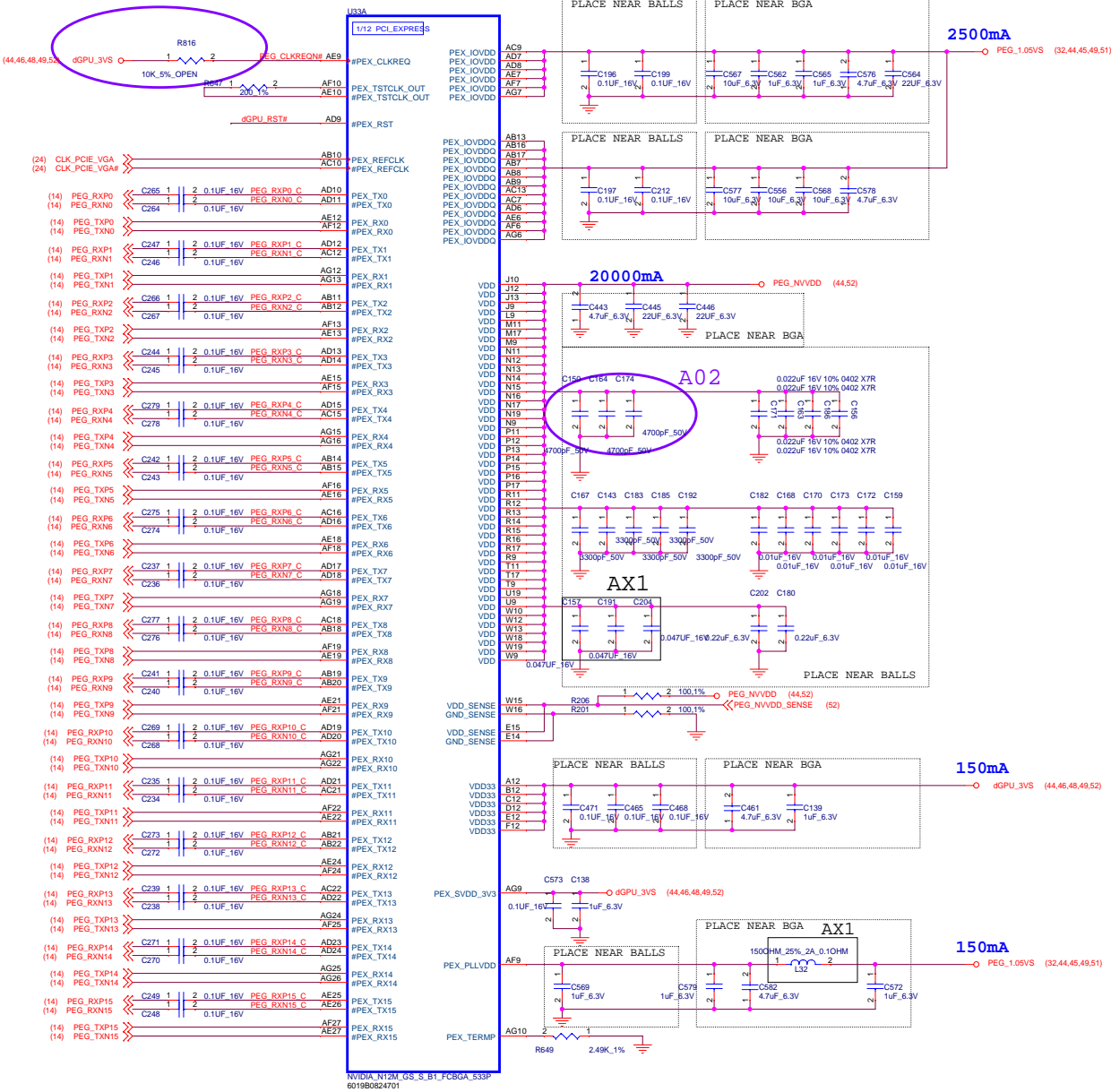
Bluetooth CNN.



PCIE Mini Card(WLAN)

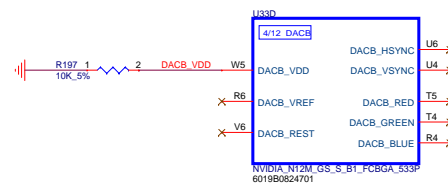
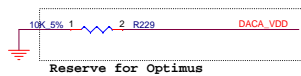
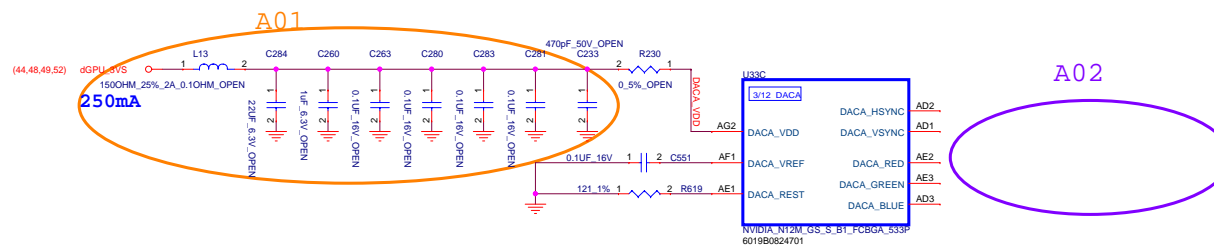


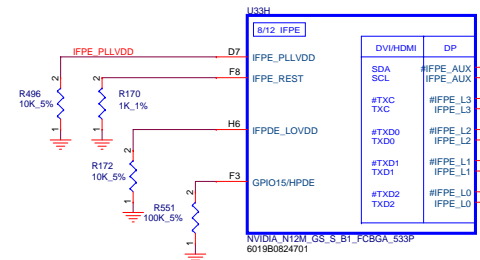
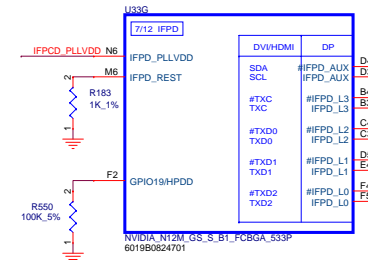
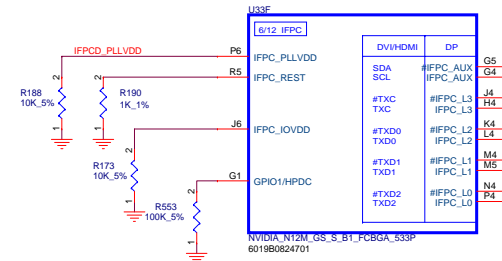
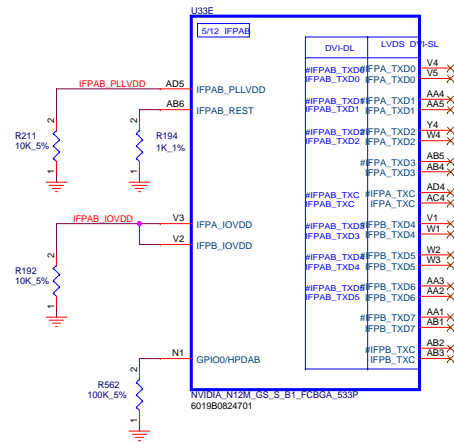
A02

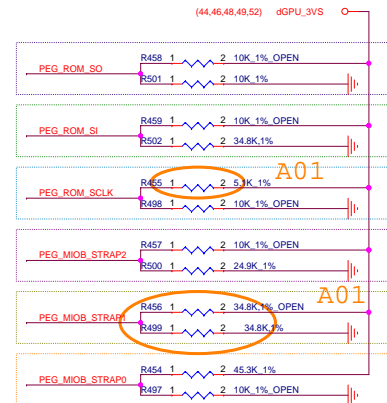
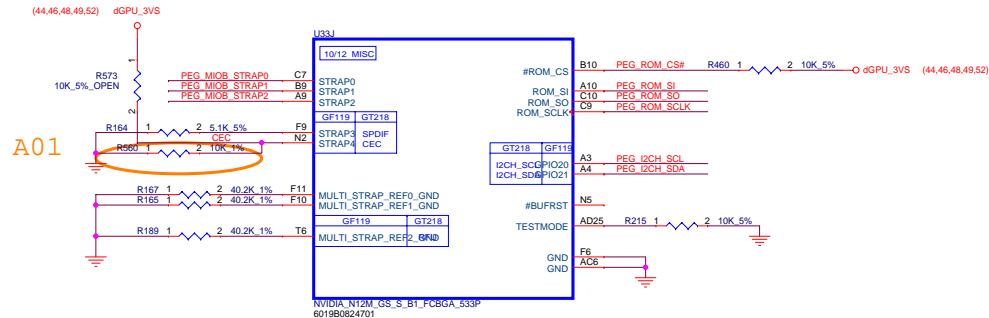


| INVENTEC | | | | |
|------------------|------|------------|-----|--|
| Strike | | | | |
| N12M/PCI-EXPRESS | | | | |
| SIZE | CODE | DOC NUMBER | REV | |
| Custom | CS | CS-131 | A02 | |
| SHEET | | 44 | of | |

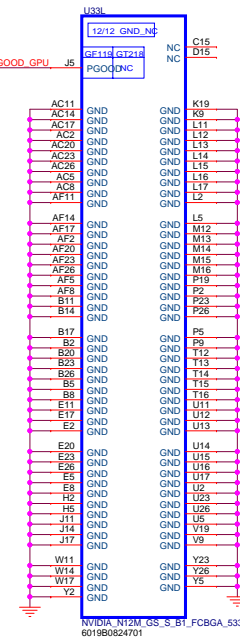
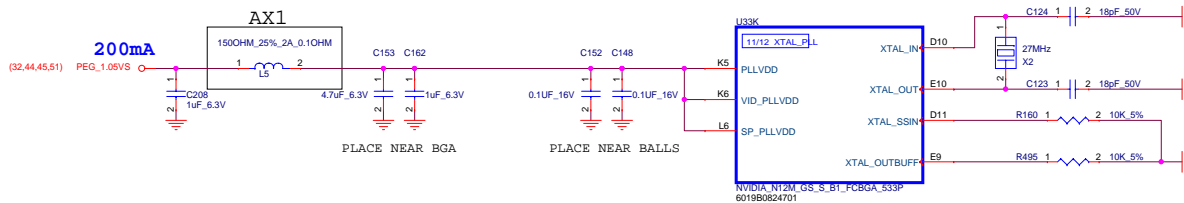
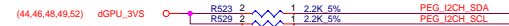
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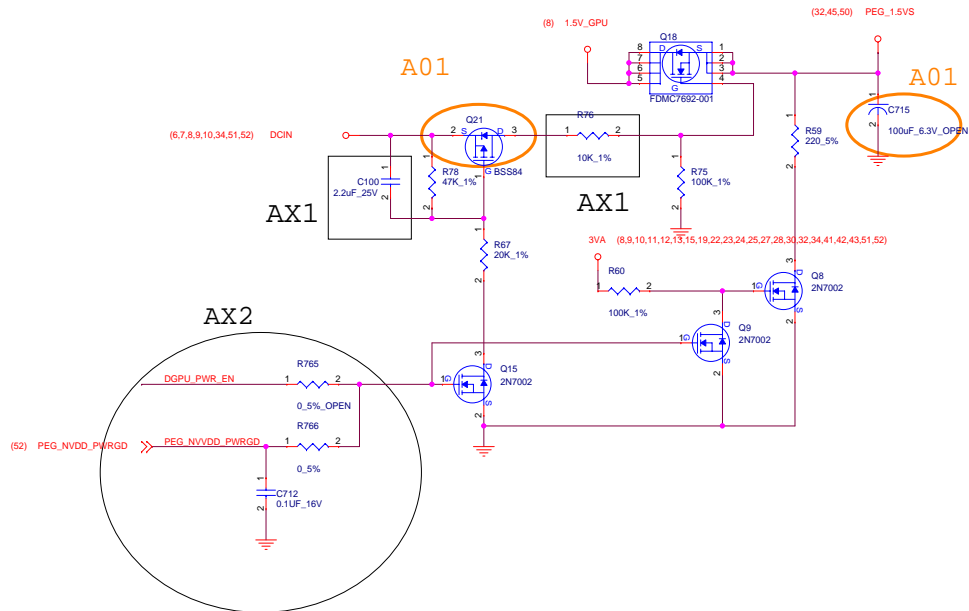
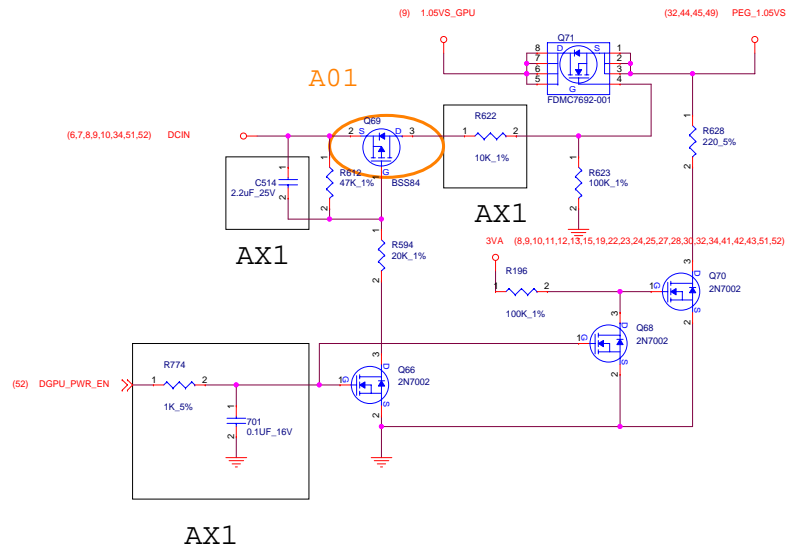
PEG_ROM_SO: PD 10K (0011)
 PEG_ROM_SI: PD 15K (0010) --> Hynix 64Kx16
 PD 20K (0011) --> Samsung 64Kx16
 PD 35K (0110) --> Hynix 128Kx16
 PD 45K (0111) --> Samsung 128Kx16
 PEG_ROM_SCLK: PU 15K (1010)
 PEG_MIOP_STRAP0: PD 35K (0100)
 PEG_MIOP_STRAP1: PD 35K (1110)
 PEG_MIOP_STRAP2: PU 45K (1111)



| Physical Trapping Pin | N11M-GE 1 Hynix H5TQ1G63BFR-12C | N11M-GE 1 SAMSUNG K4W1G1646E-HC12 | N11M-GE 2 Hynix H5TQ1G63BFR-12C | N11M-GE 2 SAMSUNG K4W1G1646E-HC12 |
|-----------------------|------------------------------------|--------------------------------------|------------------------------------|--------------------------------------|
| PEG_ROM_SO | 10K:pull-down | 10K:pull-down | 10K:pull-down | 10K:pull-down |
| PEG_ROM_SI | 15K:pull-down | 20K ohm Pull-Down | 15K:pull-down | 20K ohm Pull-Down |
| PEG_ROM_SCLK | 15K:pull-Up | 15K:pull-Up | 15K:pull-Up | 15K:pull-Up |
| PEG_MIOP_STRAP2 | 30K:pull-down | 30K:pull-down | 5K:pull-down | 5K:pull-down |
| PEG_MIOP_STRAP1 | 35K:pull-up | 35K:pull-up | 35K:pull-up | 35K:pull-up |
| PEG_MIOP_STRAP0 | 45K:pull-up | 45K:pull-up | 45K:pull-up | 45K:pull-up |

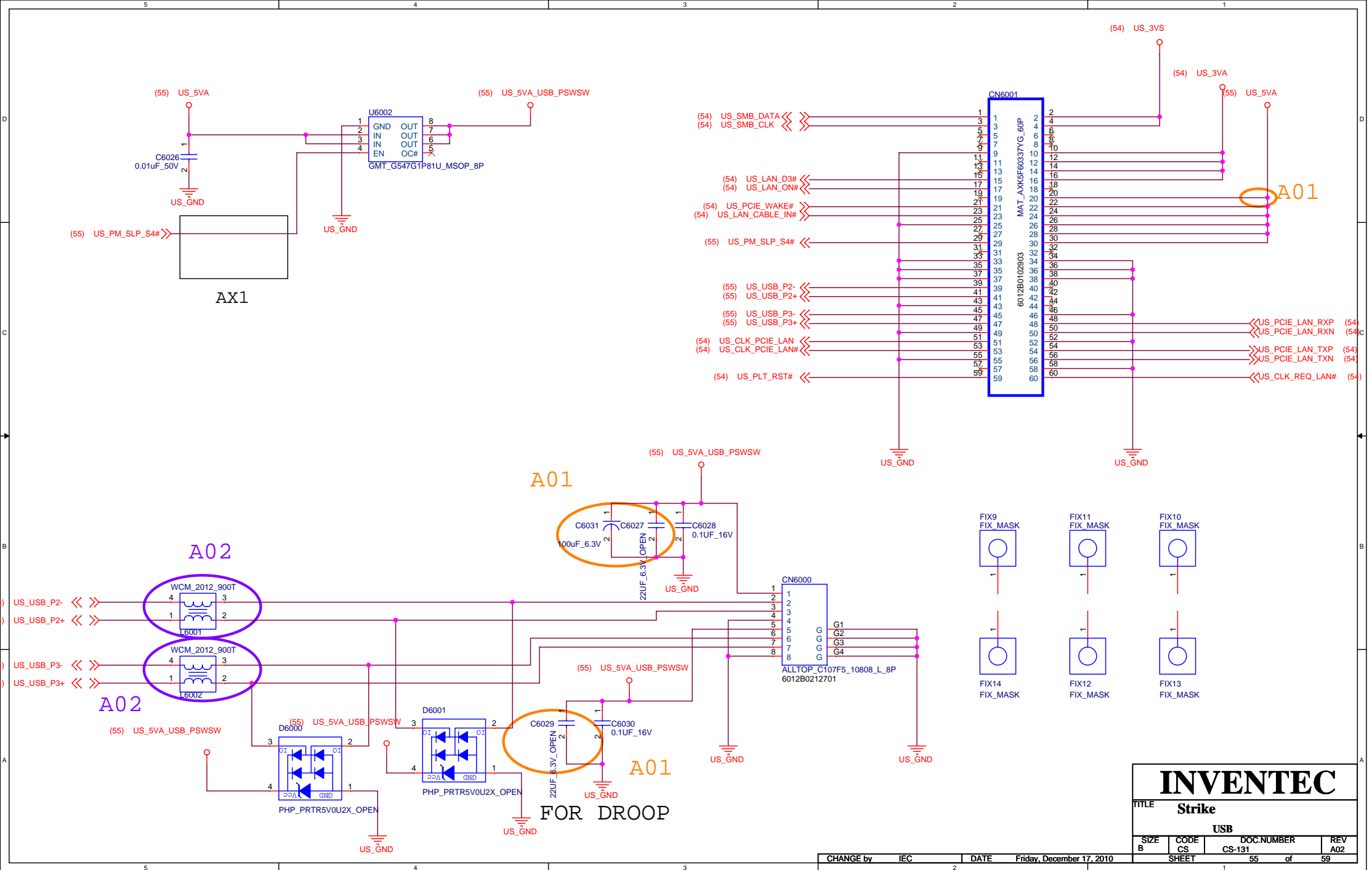
| Device | Interface | I2C Bus |
|--------|-----------|----------|
| CRT | DAC A | I2C A |
| LVDS | LVDS | I2C C |
| DVI | IFP C | IFPC_AUX |

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Strike USB Board

2010.12.15

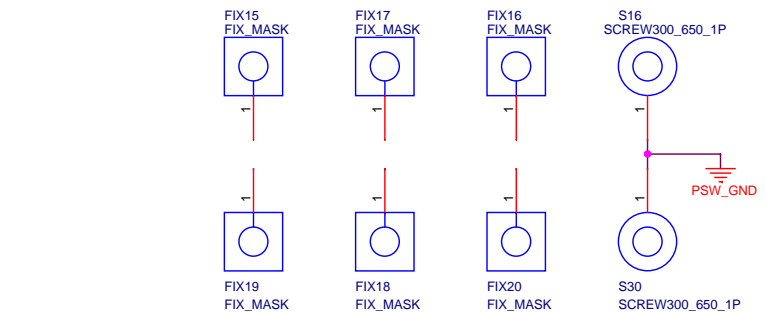
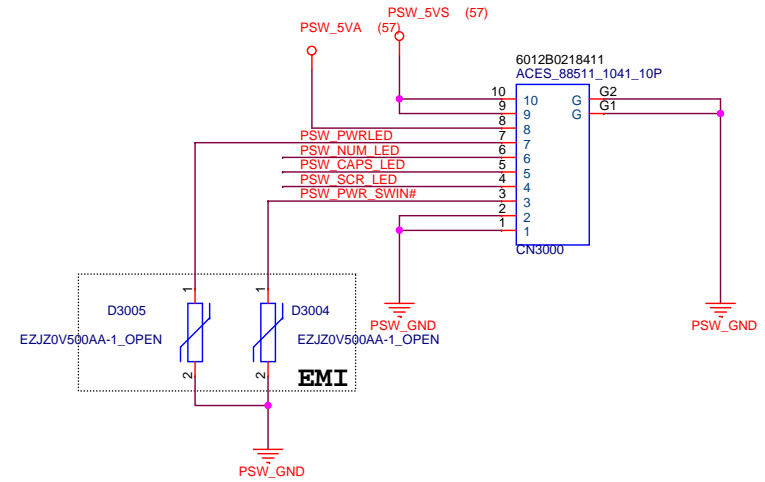
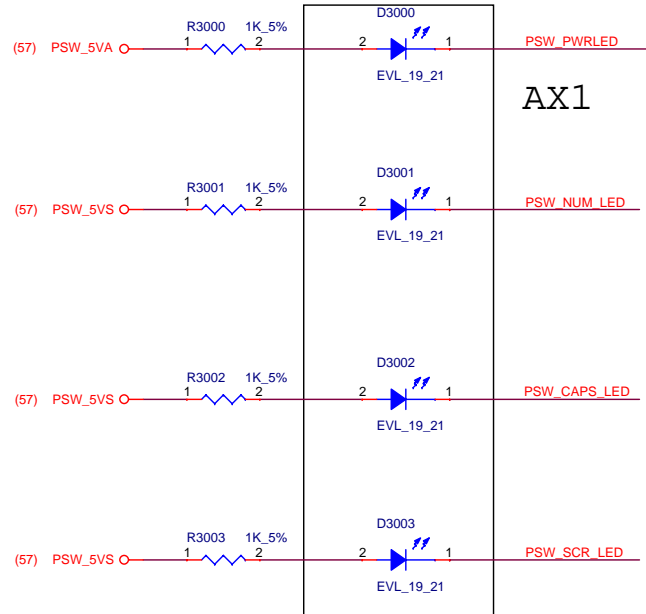
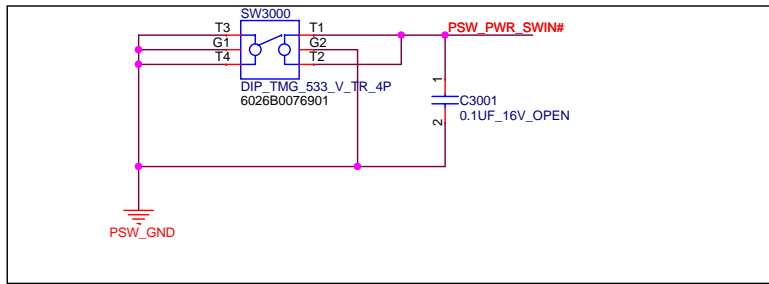


Strike

PWR_SW BOARD

2010.12.15

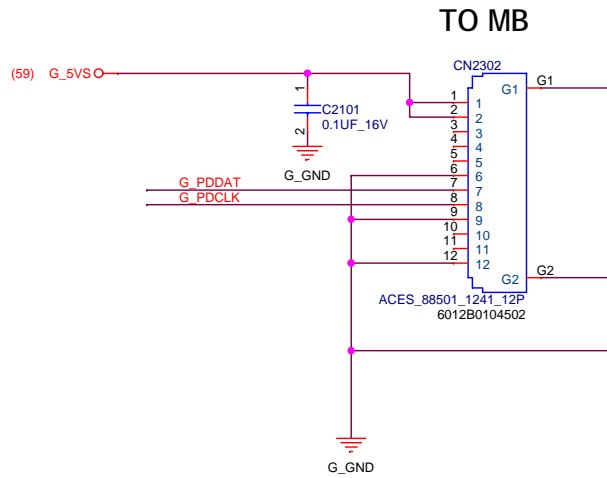
AX1



| INVENTEC | | | |
|---------------------------|---------|--------------------------------|----------------|
| TITLE Strike Power Switch | | | |
| SIZE B | CODE CS | DOC NUMBER K-CS-1310A22219-ALG | REV A05 |
| CHANGE by BEN LEE | | DATE Friday, December 17, 2010 | SHEET 57 of 59 |

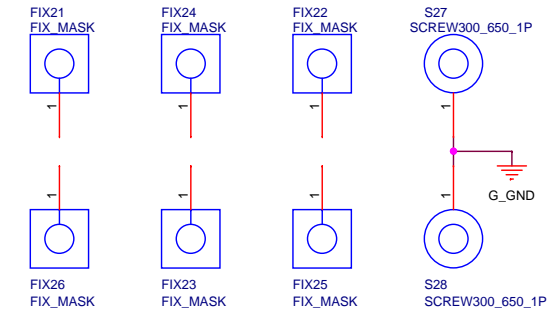
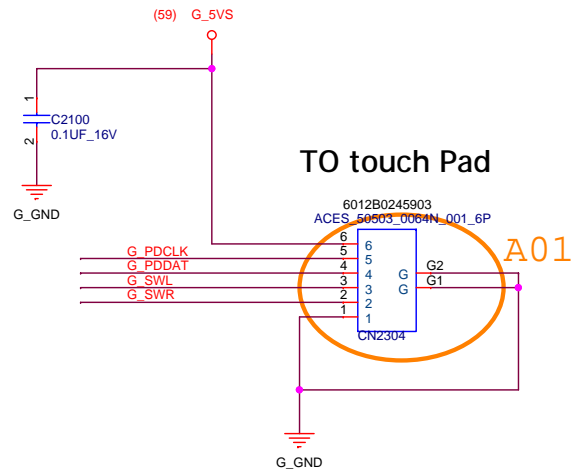
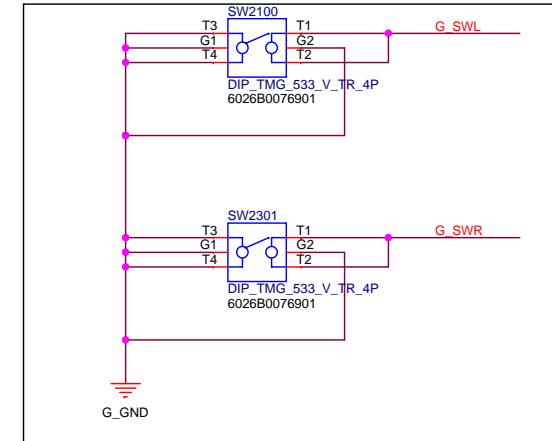
Strike GP board

2010.12.15



GP Button

AX1



INVENTEC

| TITLE | | | |
|------------------|------|-----------------|-------|
| Strike GP CNN | | | |
| SIZE | CODE | DOC NUMBER | REV |
| B | CS | K-CS-1310A22499 | A02 |
| SHEET | | 59 | of 59 |

CHANGE by CY DATE Friday, December 17, 2010